1541 Single Drive Floppy Disk
MAINTENANCE MANUAL

Michael G Peltier

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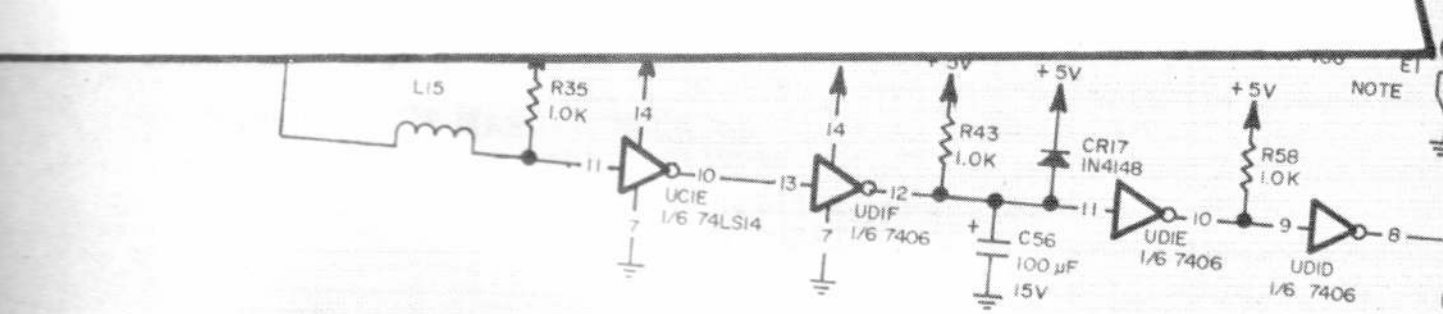

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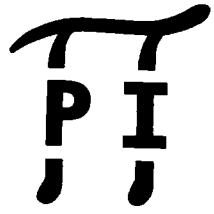

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The information in this manual has been reviewed and is believed to be entirely correct. No responsibility, however, is assumed for any personal or property damage incurred from the use of this manual. The material in this manual is for information purposes only, and is subject to change without notice.

WARNING:

HIGH VOLTAGE EQUIPMENT

THIS EQUIPMENT CONTAINS CERTAIN CIRCUITS AND/OR COMPONENTS OF EXTREMELY HIGH VOLTAGE POTENTIALS, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. WHEN PERFORMING ANY OF THE PROCEDURES CONTAINED IN THIS MANUAL, HEED ALL APPLICABLE SAFETY PRECAUTIONS.

RESCUE OF SHOCK VICTIMS

1. DO NOT ATTEMPT TO PULL OR GRAB THE VICTIM
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER.
3. IF YOU CANNOT TURN OFF ELECTRICAL POWER, PUSH, PULL OR LIFT THE VICTIM TO SAFETY USING A WOODEN POLE, A ROPE OR SOME OTHER DRY INSULATING MATERIAL.

FIRST AID

1. AS SOON AS VICTIM IS FREE OF CONTACT WITH SOURCE OF ELECTRICAL SHOCK, MOVE VICTIM A SHORT DISTANCE AWAY FROM SHOCK HAZARD.
2. SEND FOR DOCTOR AND/OR AMBULANCE.
3. KEEP VICTIM WARM, QUIET AND FLAT ON HIS/HER BACK.
4. IF BREATHING HAS STOPPED , ADMINISTER ARTIFICIAL RESUSCITATION. STOP ALL SERIOUS BLEEDING.

ACKNOWLEDGEMENTS

The author wishes to take this opportunity to thank the reader for selecting this manual. It is hoped that the information contained herein will enable the reader to fully utilize the potential of the VIC-1541. Inquiries about the manual may be directed to:

PELTIER INDUSTRIES
735 N. Doris
Wichita, Kansas 67212

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APPENDICES

SECTION 1
INTRODUCTION

Section 1-INTRODUCTION

1-1. General

This manual is produced with the amateur technician in mind. Required equipment is held to a necessary minimum in all cases. The technician should read and understand Section 2-THEORY OF OPERATION before attempting repair of the VIC-1541. Prior to attempting any procedure in this manual, the procedure must be read and understood. The general flow of procedures used in isolating and repairing a problem is given in Figure 1-1.

1-2. Electrical

The VIC-1541 contains the following major electrical assemblies:

Frame-contains power regulation and distributes power throughout unit.

Drive Unit-contains the Drive Motor Servo circuit and the Read/Write heads.

Disk Controller PC Board-contains Timing, Track Select, Write, Read, Encoder/Decoder, Optics and Computer circuits.

1-3. Mechanical

The VIC-1541 contains the following major mechanical assemblies:

Case-includes top cover and bottom cover.

Drive Unit-contains,as one replaceable assembly, the drive motor, timing drive and all mechanical parts for acting upon a floppy disk.

Frame-consists of a metal tray, a transformer and various plugs.

Disk Controller PC Board-a large PC Board located on top of the frame.

RFI Shield-a large metal cover that protects the components on the Disk Controller PC Board.

1-4. Warnings, Cautions and Notes

Throughout this manual are a number of Warnings, Cautions and Notes. A Warning means that there is a possibility of serious injury, or even death, to the technician if the Warning is not heeded. A Caution means that there is a possibility of damage to the VIC-1541 if the Caution is not heeded. A Note is intended to serve as an aid to the technician in understanding text or in following a procedure.

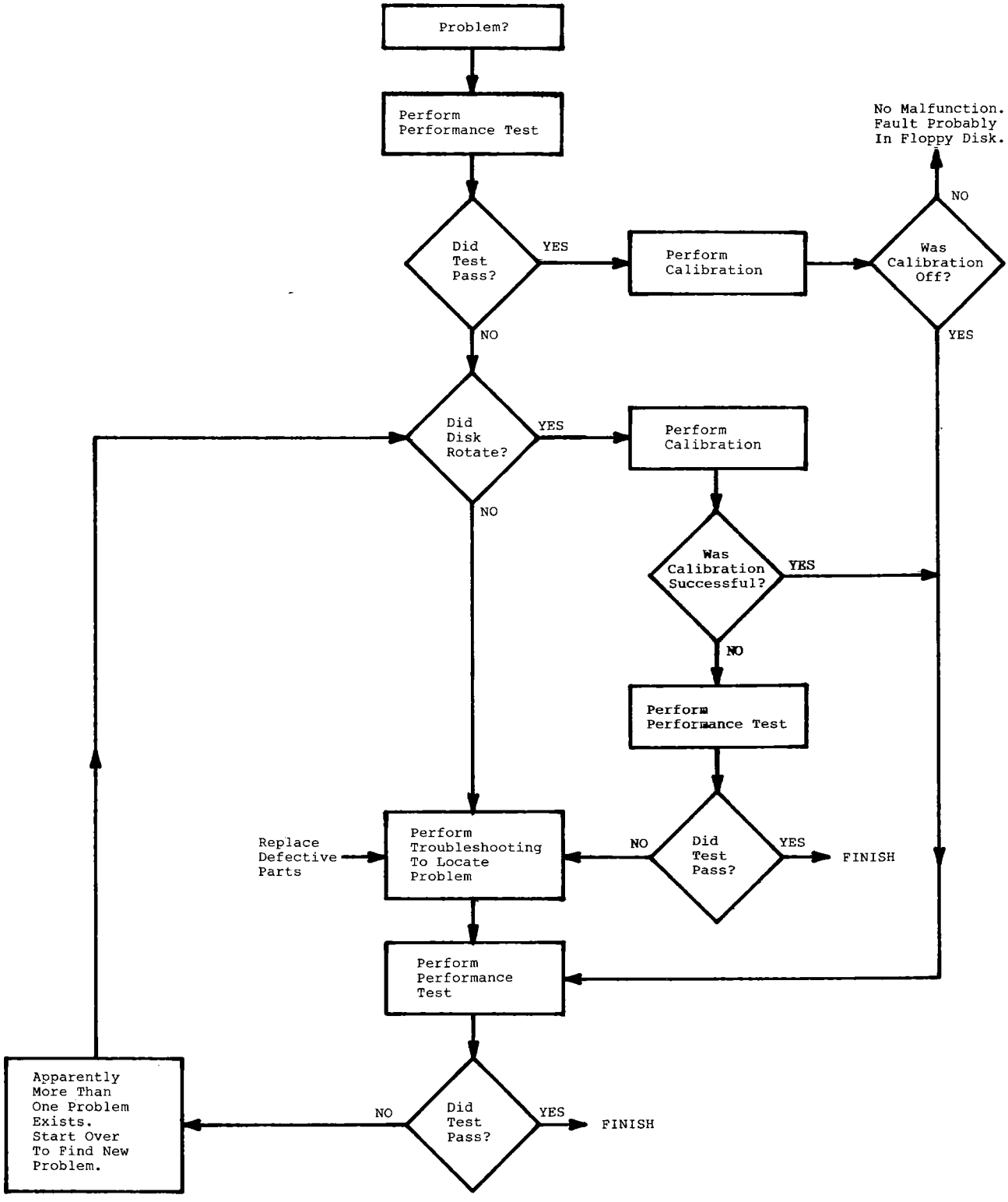


Figure 1-1. How-To-Use Manual Flowchart.

SECTION 2
THEORY OF OPERATION

Section 2-THEORY OF OPERATION

2-1. Overall Theory

The VIC-1541 consists mainly of three sub-assemblies: disk controller PC Board, drive unit and frame.

The frame sub-assembly provides the power supply on the drive controller PC Board with +9 Vrms and +16 Vrms, which are derived from the 115 VAC or 230 VAC power input. (Refer to Section 3 for selection of input power.)

The drive unit sub-assembly is capable of reading or writing to or from a floppy disk. The drive unit is also capable of rotating the floppy disk, changing read/write head location, detecting write protect status, and magnetically reading or writing data.

The disk controller PC Board sub-assembly includes the power supply, read/write circuitry, track select circuitry, timing circuitry, and a 6502-based computer. The computer operates the drive unit as well as managing the floppy disk. The program which this computer uses is called the DOS (Disk Operating System).

The floppy disk consists of a mylar disk with a magnetic coating inside a jacket (Refer to Figure 2-1). The jacket has several cutouts in it. The index cutout (Item 1) is not used in the VIC-1541 since sector information is written on each block. The slot (Item 2) allows the head to touch the magnetic coating. A similar slot is cut on the opposite side of the floppy disk. The write protect slot (Item 3) is provided as a means of protecting a disk against accidental erasure or overwriting. If the write protect slot is left uncovered, writing to the floppy disk is permitted. If the write protect slot is covered with opaque tape, writing is disabled.

The recording principles involved are identical to those of magnetic tape. The shape of the disc is more convenient than magnetic tape since each piece of information passes the vicinity of the head three hundred times per minute. This allows random access of the information on the disk. Data is physically stored in rings on the face of the disk. These rings are called tracks. There are 35 tracks on each disk. Each track is further divided into sectors. Each sector contains sync, ID, track, sector and checksum information along with 254 bytes of data. Track #18 is used for housekeeping purposes (i.e., the directory and the block availability map). Track #18 is automatically managed by the DOS. Any information to be written or read is received and transmitted by the disk controller to the VIC-20/COMMODORE 64 over the serial bus.

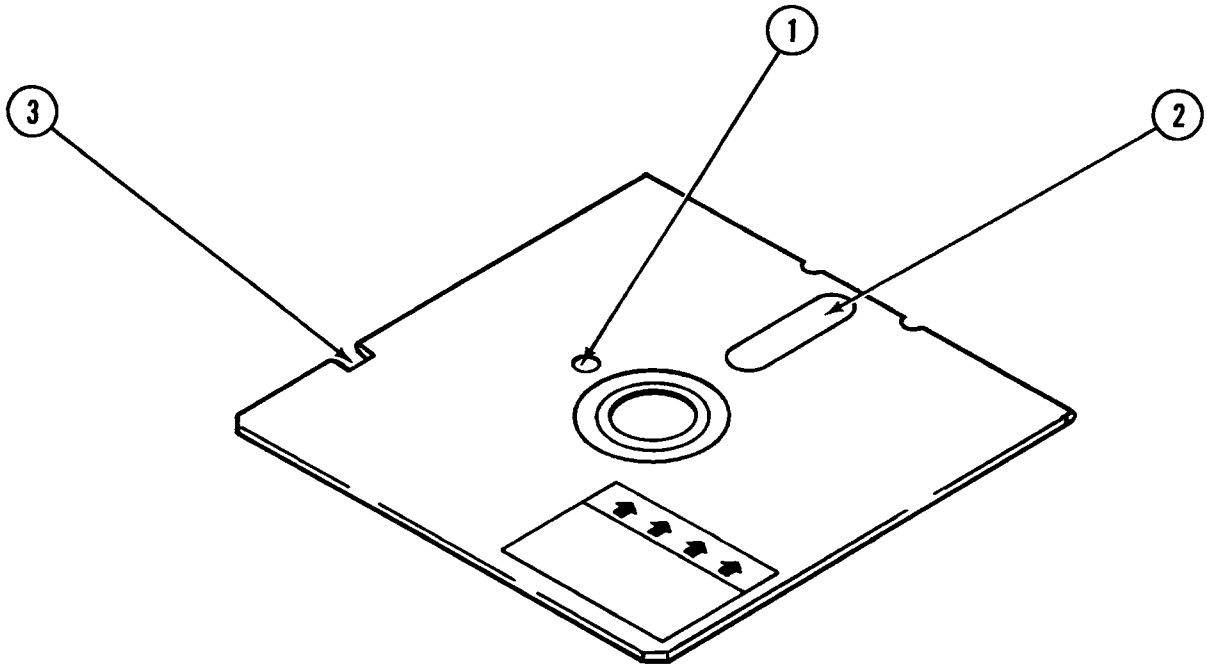


Figure 2-1. Floppy Disk

2-2. Mechanical Theory

2-2-1. Loading and Unloading (Refer to Figure 2-2)

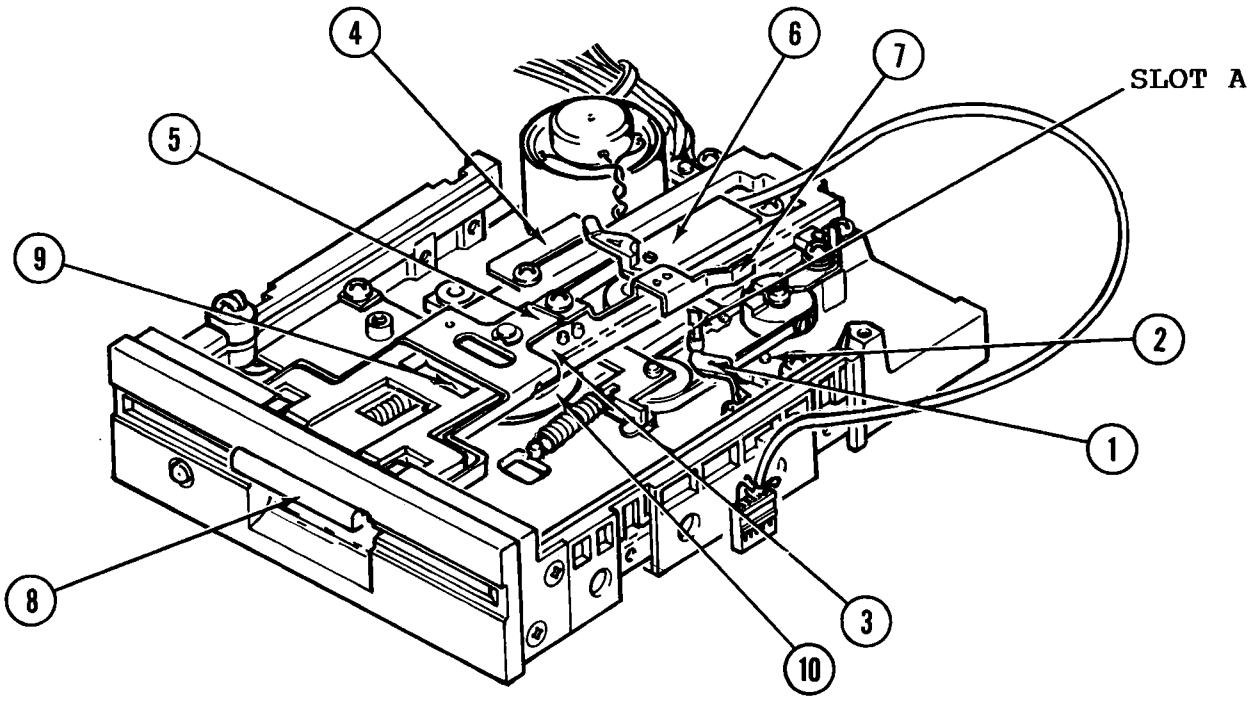


Figure 2-2. Drive Unit, Loading and Unloading.

Every time a floppy disk is inserted into the VIC-1541 drive unit, four things happen:

1. The disk ejector is cocked.

2. Read/write head pressure is applied.

3. Disk tension is set.

4. The disk is held firmly against the drive hub.

When a disk is inserted into the drive unit, the disk will push back on the disk ejector arm (Item 1) until it reaches the ejector arm pin (Item 2) which holds the disk ejector arm in the cocked position.

After the disk is inserted, the idler hub mount (Item 3) is pressed down. As the idler hub mount is depressed, several other actions occur. The disk tension pad (Item 4) is moved into place, setting the disk tension. The unloading actuator (Item 5) is lowered, allowing the pressure pad mount (Item 6) to be lowered onto the disk, setting the read/write head pressure. As the idler hub mount nears its seated position, the disk ejector trigger (Item 7) on the unloading actuator

falls into slot A of the disk ejector arm. When the idler hub mount is fully seated, the latch (Item 8) retains the idler hub mount in its seated position. In this seated position, the idler hub (Item 9) sandwiches the media between it and the drive hub (Item 10). The floppy disk is then ready to be accessed.

To unload the floppy disk, the latch is pressed, allowing the idler hub mount to pop up. As the idler hub mount is moving upwards, the disk tension pad is raised, removing the disk tension. The unloading actuator is also raised, lifting the pressure pad mount and tripping the disk ejector arm. The disk ejector arm then moves up over the ejector arm pin and kicks the floppy disk approximately 1 to 2 inches out the front of the drive unit.

2.2.2. **Track Selection** (Refer to Figure 2-3)

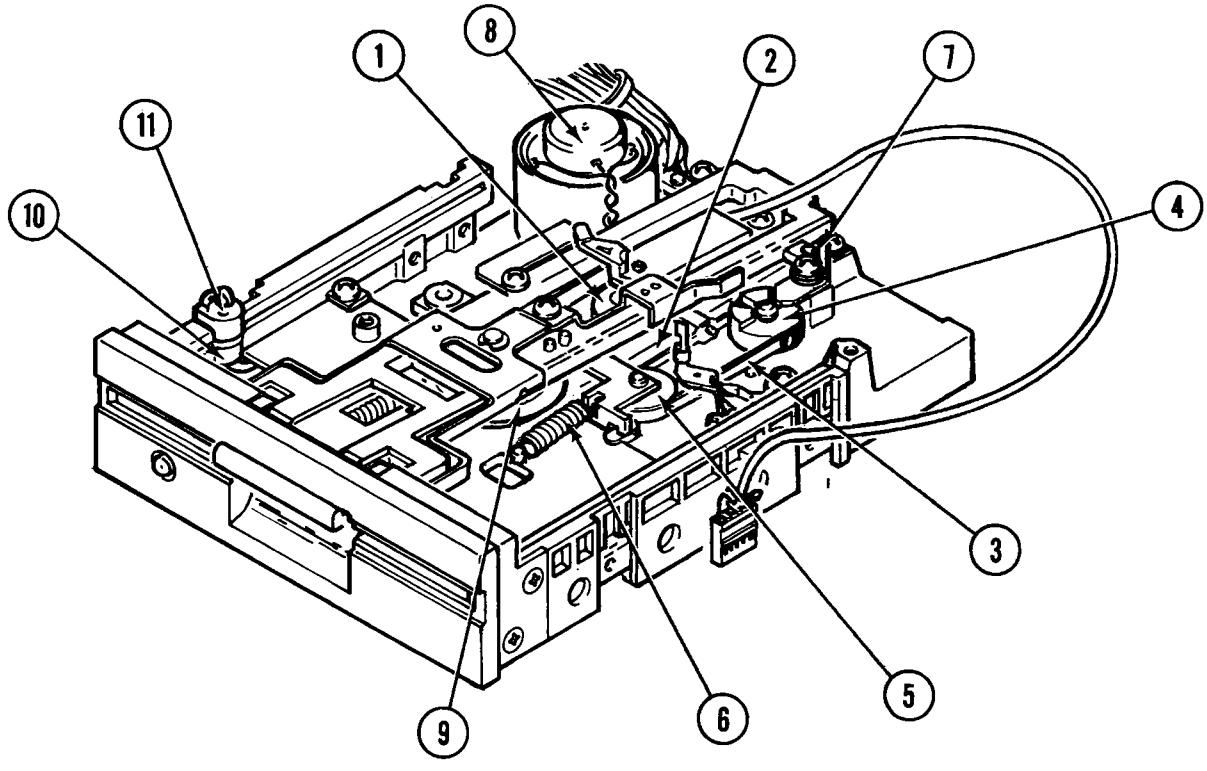


Figure 2-3. Drive Unit, Track Selection and Write Protect.

The mechanical track selection system allows the position (inward-outward position) of the heads to be selected. The read/write head mount (Item 1) can move front to back on the head mount side rails (Item 2). The read/write head mount is attached to the track selct band (Item 3). The track select band is secured to the stepping motor drive wheel (Item 4) and wrapped around the track position idler pulley (Item 5). The tension of the track position idler pulley and of the track select band is set by a spring (Item 6). The stepping motor (Refer to Figiure 2-4, Item 1) rotates in 1.8 degree

increments. As the stepping motor drive wheel rotates, the track selct band also rotates, causing the read/write head mount to move inward or outward. Overrunning the outermost track is prevented by the stepping motor stop (Item 7).

2-2-3. **Drive System** (Refer to Figure 2-4)

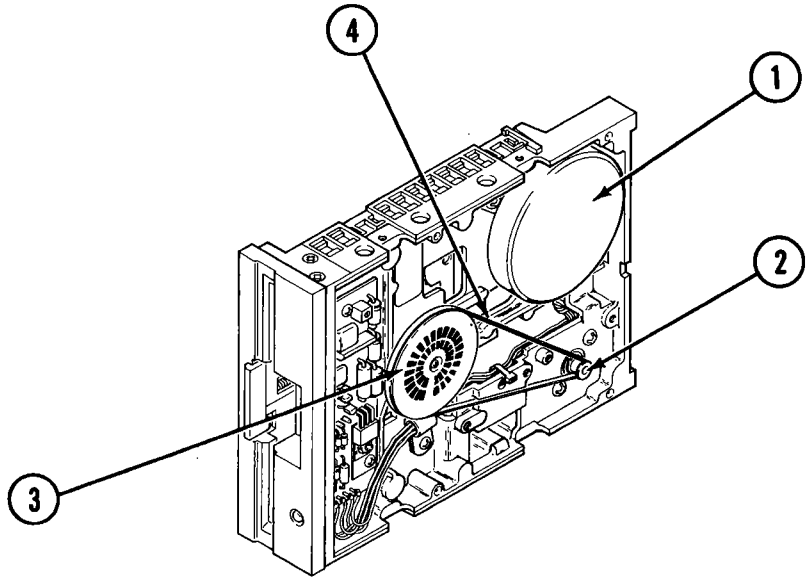


Figure 2-4. Drive Unit, Drive System.

The mechanical drive system rotates the drive hub and thus the disk itself. The drive motor/tachometer (Figure 2-3, Item 8) contains a motor and a tachometer on a common shaft. The tachometer is used to generate speed information for feedback purposes. The drive motor shaft is connected to the drive pulley (Item 2), which turns the flywheel (Item 3) via the drive belt (Item 4). The flywheel smooths out the motion of the drive hub (Figure 2-3, Item 9). The flywheel also contains a timing disk for the purpose of disk speed calibration.

2-2-4. **Write Protect System** (Refer to Figure 2-3)

The write protect system consists of an LED (Item 10) and a phototransistor (Item 11). When a floppy disk is inserted with the write protect notch uncovered, the LED transmits light to the phototransistor, activating the phototransistor. The phototransistor then informs the disk conroller that writing to the disk is permitted. If, however, the write

protect notch is covered, the light beam is interrupted and the disk controller will not permit writing to the floppy disk.

2-3. **Electrical Theory** (Refer to Figures 2-5 and 2-6)

2-3-1. **Frame Electrical Theory**

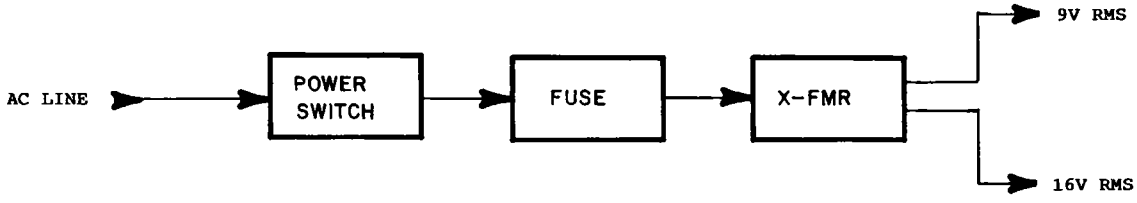
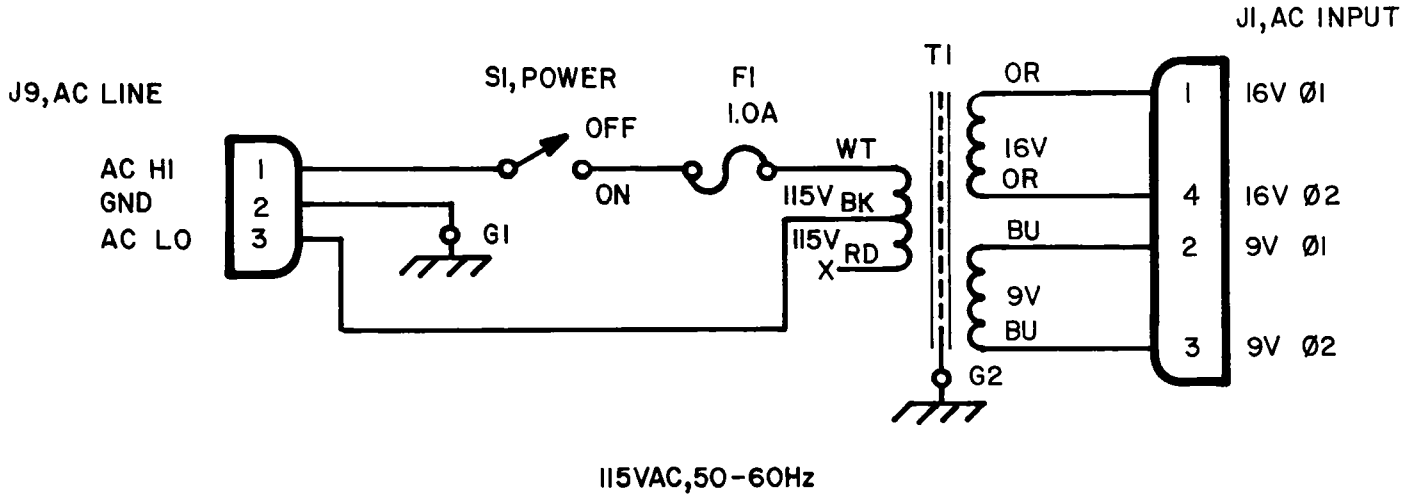


Figure 2-5. Frame Assembly, Block Diagram.

The electrical function of the frame assembly is to condition and convert the AC line voltage before applying it to the power supply on the disk controller PC Board.

The AC line voltage enters the disk drive at J9, which is both a connector and an RFI filter. After passing through the filter, the AC voltage is applied to the SPST power switch, S1. The output of the power switch is applied to F1, which provides over-current protection. F1 is a 1A fuse for 115 VAC operation and a 0.5A fuse for 230 VAC operation. The output of F1 is fed to the transformer, T1. T1 steps down the AC line voltage into +9 Vrms and +16 Vrms. Both of these outputs have their own secondary windings and are isolated from each other.

It should be noted that the AC return line for the primary of T1 may be connected to either tap on the primary winding. With the black tap connected, the disk drive is configured for 115 VAC @ 50-60 Hz operation. With the red tap connected the disk drive is configured for 230 VAC @ 50-60 Hz operation.



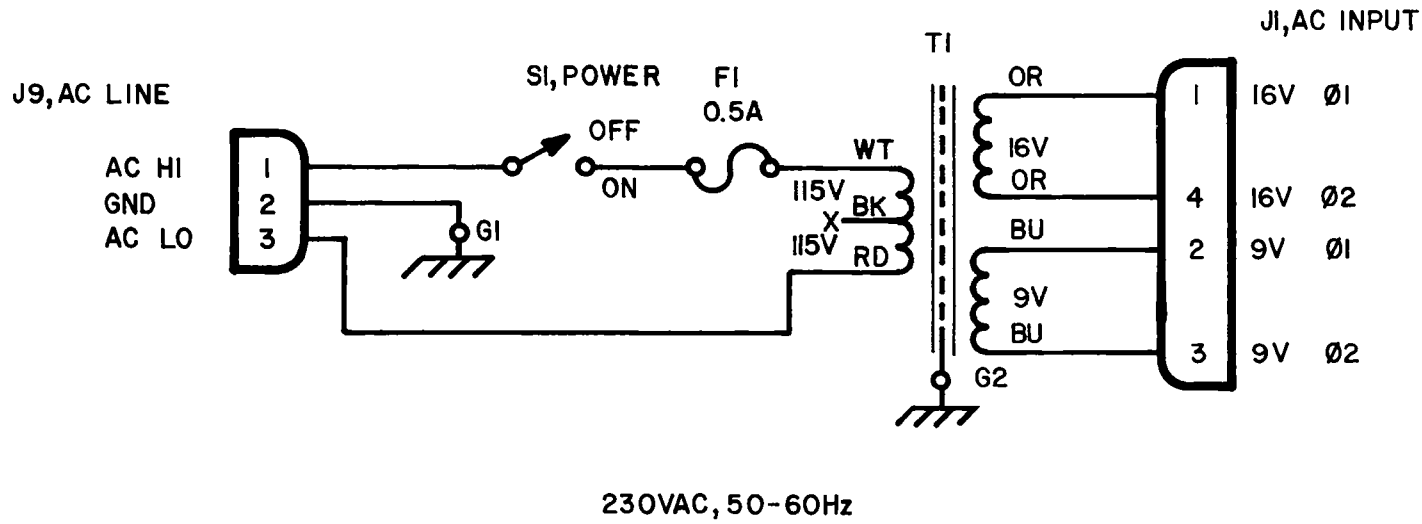


Figure 2-6. Frame Assembly, Schematic.

CAUTION

- NEVER CONNECT BOTH TAPS AT THE SAME TIME.

Always properly insulate the disconnected tap with electrical tape or heat shrink tubing (Refer to Section 3 for initial configuration of the disk drive).

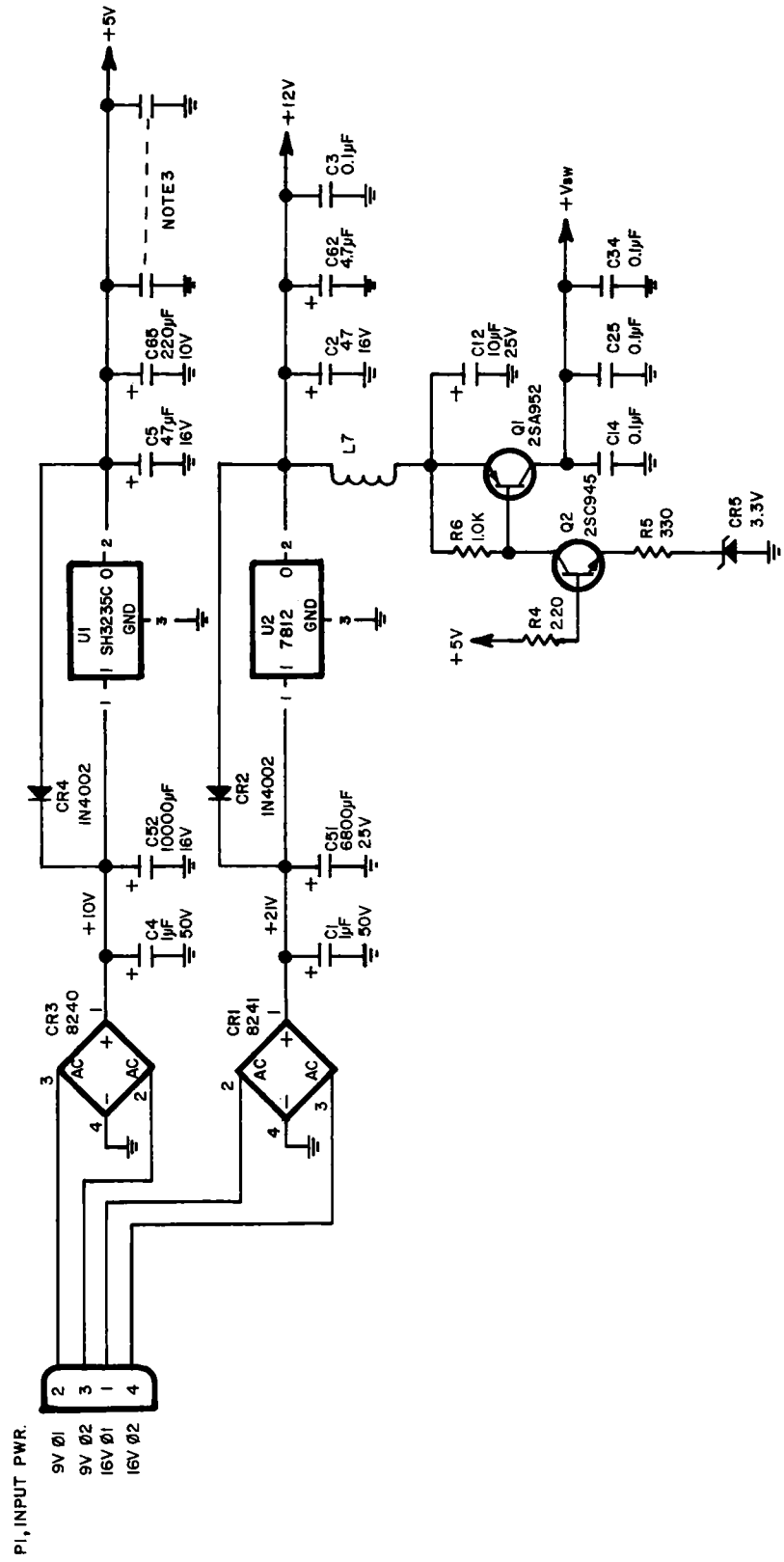


Figure 2-7. Power Supply, Schematic.

2-3-2. **Power Supply Electrical Theory** (Refer to Figures 2-7 and 2-8)

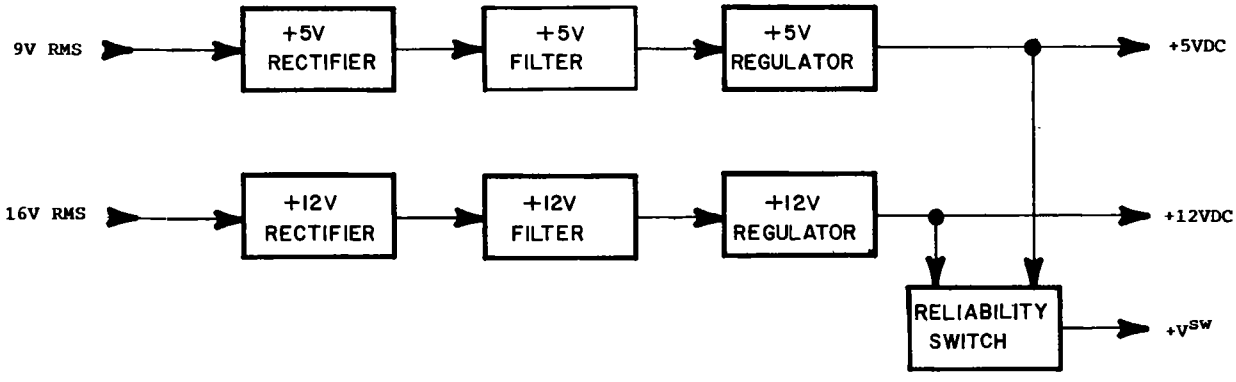


Figure 2-8. Power Supply, Block Diagram.

The VIC-1541 power supply produces two regulated voltages, +12 VDC and +5 VDC. These voltages are derived, respectively, from the +16 Vrms and +9 Vrms supplied by the frame assembly. The power supply, located on the disk controller PC Board, has a reliability switch which removes power from the write amplifiers in the event of a +5 V failure or during power up/down. Thus, the reliability switch protects the data on the floppy disk by disabling the write amps whenever the +5 V line goes below 3.9 V.

1. +12 VDC.

16 Vrms is applied to the power supply via pins 1 and 4 of P1. From P1 the AC power is applied to bridge rectifier CR1. CR1 rectifies (full wave) the +16 Vrms to produce approximately +21 VDC. The output of the rectifier is applied to a filter consisting of C1 and C51, which smooths out the pulsating DC from CR1. The output of the filter is applied to U1, a +12 V regulator. The output of U1 is the regulated +12 VDC output of the power supply. C2, C62 and C3 reduce line noise and CR2 protects the regulator against negative voltage excursions during power up/down.

2. +5 VDC.

The +5 V leg of the power supply operates in the same fashion as the +12 V leg, the only difference being voltage levels. +9 Vrms is applied to the power supply via pins 2 and 3 of P1. The AC power is applied to bridge rectifier CR3. After rectification, the resulting +10 VDC is filtered by C4 and C52 before it is applied to the +5 V regulator, U2. The output of U2 is the regulated +5 VDC output of the power supply. C5 and C65 reduce line noise and CR4 protects the regulator against negative voltage excursions during power up/down.

3. Reliability Switch.

The reliability switch consists of Q1, Q2, CR5 and associated components. Q2 and CR5 form a comparator. When the +5 V line exceeds +3.9 V, base current of Q2 flows through the base-emitter junction via R4, R5 and CR5. The cutoff voltage is determined by CR5 (3.3 V) and the base-emitter drop of Q2 (0.6 V). As base-emitter current increases, collector-emitter current also increases. When Q2 begins to draw collector current, it forces Q1 into conduction by causing base-emitter current to flow through Q1 via L7, Q2, R5 and CR5. When Q1 is turned on, approximately 11.6 V is applied to the $+V_{SW}$ line to enable the write amplifiers. If the +5 V line drops below 3.9 V, Q2 is turned off, in turn turning off Q1. With Q1 turned off, power is removed from the $+V_{SW}$ line and the write amplifirs are disabled. R6 ensures proper turn-off of Q1 by shunting any Q2 leakage current away from Q1. L7 and C12 form a lowpass L-type filter which isolates the noise produced by the motors in the +12 V line. C14, C25 and C34 are bypass capacitors which reduce noise in the $+V_{SW}$ line.

2-3-3. **Timing Electrical Theory** (Refer to Figures 2-9 and 2-10)

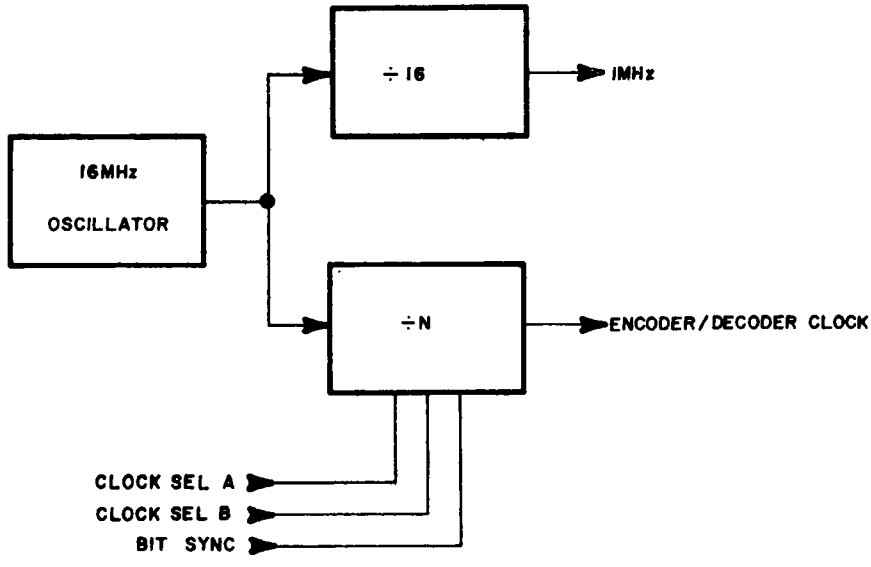


Figure 2-9. Timing Circuit, Block Diagram.

The timing circuit produces the clock signals. One of the outputs is a 1 MHz square wave. This fixed 1 MHz clock signal is applied to the microprocessor, controlling the rate at which the microprocessor executes instructions. The second output is a variable frequency square wave which is used to control the Encoder/Decoder circuit. The timing circuit consists of a 16 MHz Oscillator, a Divide-by 16 Frequency Divider and a Programmable Divider.

1. 16 MHz Oscillator.

The 16 MHz Oscillator consists of UC7, Y1 and associated components. Y1, UC7C, UC7D, R1, R2 and C10 form a crystal-controlled square wave oscillator. UC7B buffers and shapes the clock signal. The output of the 16 MHz oscillator (UC7B,pin4) is applied to the Divide-by 16 Frequency Divider and to the Programmable Divider.

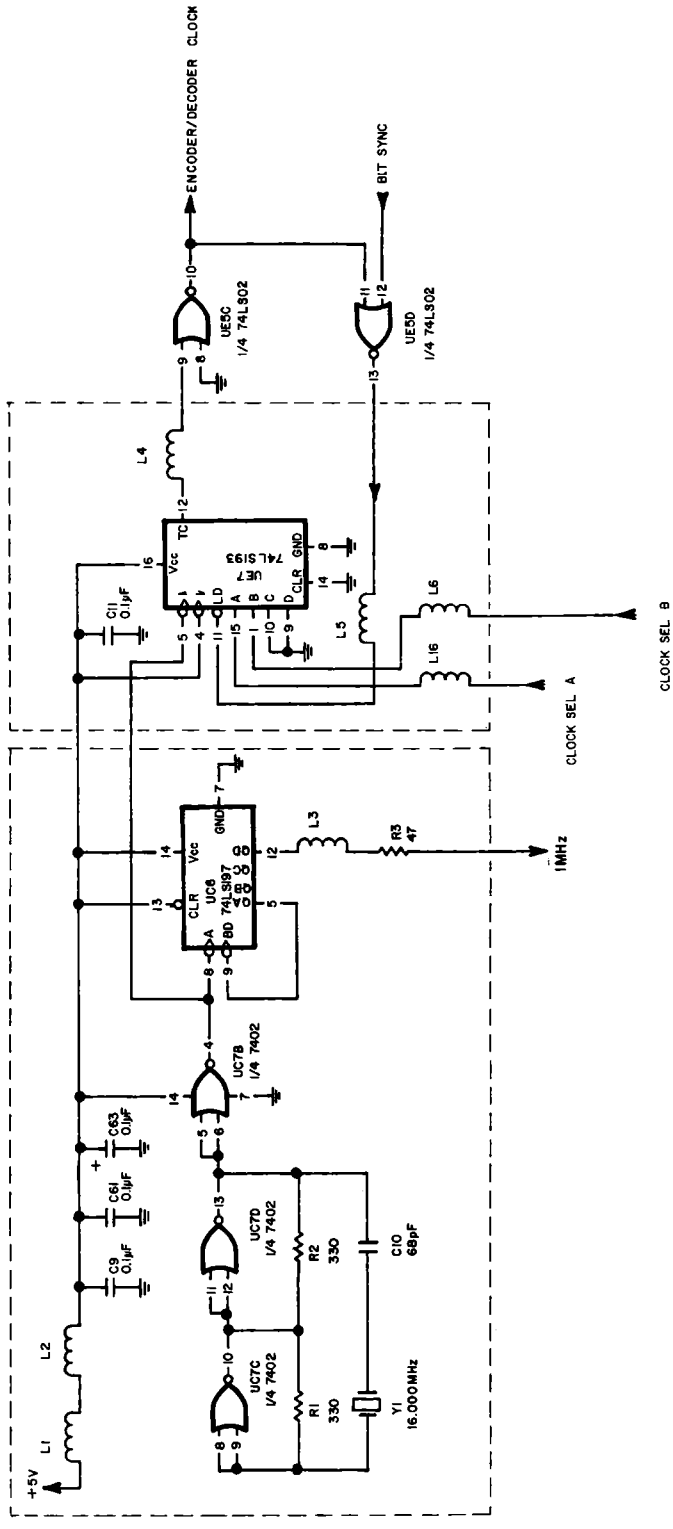


Figure 2-10. Timing Circuit, Schematic.

2. Divide-by 16 Frequency Divider.

The Divide-by 16 Frequency Divider consists of a four bit binary counter, UC6. Pin 5 (the divide-by 2 output) of UC6 is applied to pin 6 of UC6 in order to clock the last three stages of the counter. The output of the Divide-by 16 Frequency Divider is taken from pin 12 and is applied to the microprocessor via L3 and R3, which filter the clock line to reduce noise.

3. Programmable Divider.

The Programmable Divider produces the clock for the Encoder/Decoder circuit and may be reset to allow the phase of the ENCODER/DECODER Clock to be controlled. Floppy disks have fewer sectors per track on the innermost track (track 35) than on the outermost track (track 1). This variation in number of sectors per track keeps the bit density fairly constant throughout the writing surface of the disk. Each disk is further divided into four zones, with each zone containing a unique number of sectors per track. The Programmable Divider has four possible output frequencies, with each frequency corresponding to one of the four zones on the floppy disk. In order to maintain fairly even bit densities, the Encoder/Decoder must be clocked at a faster rate when writing on the outer tracks than when writing on the inner tracks. This is because the outer surface of the disk is passing over the head more quickly than the inner surface. Thus, it is the ENCODER/DECODER Clock which determines how many sectors will fit on any given track.

The division factor of the Programmable Divider is controlled by the CLOCK SEL A and CLOCK SEL B lines. The following table defines specific parameters for each zone:

	Zone 1	Zone 2	Zone 3	Zone 4
CLOCK SEL A	1	0	1	0
CLOCK SEL B	1	1	0	0
Division Factor	13	14	15	16
ENCODER/DECODER Clock Freq (MHz)	1.2307	1.1428	1.0666	1
Sectors per Track	21	20	18	17
Track Numbers	1-17	18-24	25-30	31-35

The Programmable Divider consists of UE7, UE5C and UE5D. UE7

is configured as a presettable 4 bit binary up counter. The output of UE7 is taken off pin 12, the TC output. The TC output (active low terminal count) goes low when the counter overflows from $1111_{(2)}$ to $0000_{(2)}$. This active low pulse is inverted by UE5C, producing a positive pulse. The output of UE5C is applied to UE5D and to the Encoder/Decoder circuit. The output of UE5D is an active low pulse and is applied to the load input of the presettable counter. When the load goes low, the counter is preset to the values present on the A, B, C and D lines. The C and D lines are strapped low and therefore each line is set to 0. If the A and B lines are both low (Zone 4 condition), the counter is preset to $0000_{(2)}$. Sixteen counts later the load line will reset the counter to $0000_{(2)}$. If only the A line is a logic 1 (Zone 3 condition), the counter is preset to $0001_{(2)}$ and fifteen counts later the load line will again preset the counter to $0001_{(2)}$. Note that only fifteen counts were required, since the counter had a head start of one count. If only the B line is a logic 1 (Zone 2 condition), the counter is preset to $0010_{(2)}$. The counter now has a head start of two counts and will require only fourteen counts before it is preset again. If both the A and the B lines are at logic 1 (Zone 1 condition), the counter is preset to $0011_{(2)}$. The counter now has a head start of three counts and will require only thirteen counts before it is preset again.

L16 and L4 thru L6 filter the signal lines to reduce noise. L1, L2, C9, C61, C63 and C11 form a lowpass L-type filter which prevents the coupling of noise from the timing circuit to the +5 V line and vice versa.

Pin 12 of UE5D is the BIT SYNC input. When a positive pulse is applied to pin 12, the output of UE5D (pin 13) is applied to the load line, causing the ENCODER/DECODER Clock to terminate the current cycle early and begin a new one. A pulse from the read circuit is applied to the bit sync input every time a high to low or a low to high transition occurs in the serial data on the disk. When this pulse occurs, the ENCODER/DECODER Clock is set to the beginning of its cycle and the clock is synchronized with the serial data. The timing circuit maintains the phase relationship between the serial data and the ENCODER/DECODER Clock to within 62 nS.

2-3-4. **Computer Electrical Theory** (Refer to Figures 2-11 and 2-12)

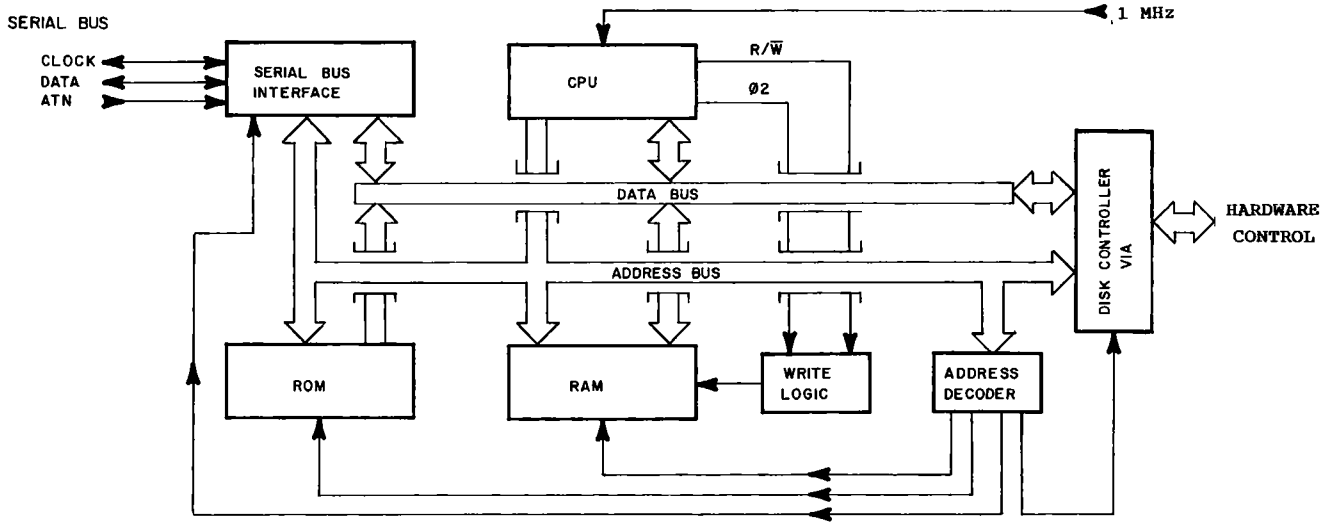


Figure 2-11. Computer, Block Diagram.

The computer performs two major functions: serial bus communication and floppy disk control. Interfacing with the serial bus is accomplished by the serial bus interface. Interfacing with the floppy disk is accomplished by the Read, Write, Track Select, Motor Drive, Timing and Optics circuits along with the Drive Unit itself. The computer communicates with these devices through the VIA (Versatile Interface Adapter). The computer consists of the MPU, ROM, RAM, write logic, address decoder, VIA and the serial bus interface.

1. MPU

UCD5 is a 6502, 8 bit microprocessor. The microprocessor fetches an instruction from ROM or RAM and executes the instruction. The instruction, in turn, causes the microprocessor to alter data in RAM, internal registers or registers in the VIAs. After completing each instruction, the MPU fetches the next instruction and the cycle continues.

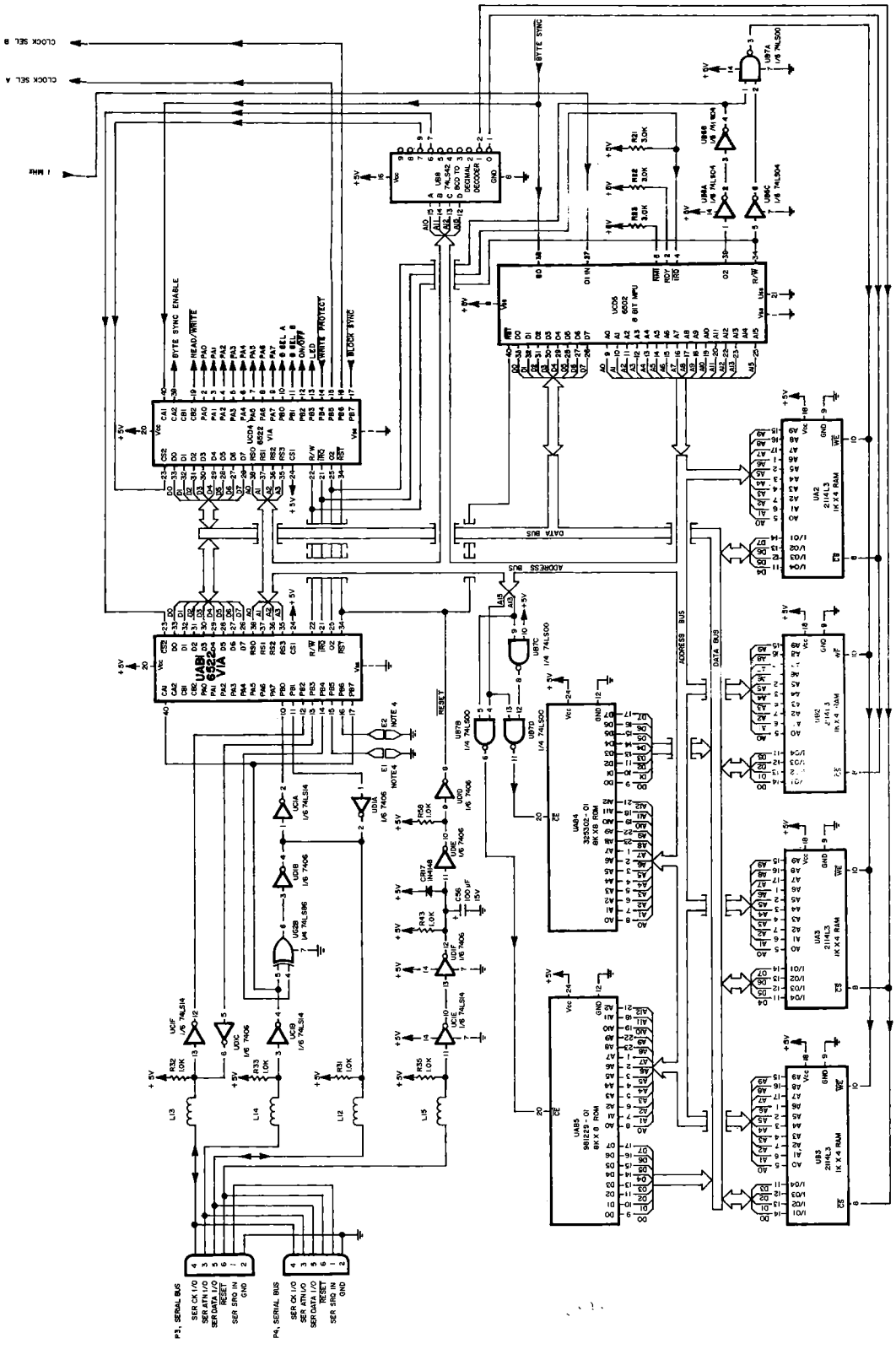


Figure 2-12. Computer, Schematic.

The rate at which the microprocessor executes instructions is determined by the θ1 Clock present at pin 37 of UCD5. The θ1 clock is produced by the Timing circuits (Refer to Timing Theory, paragraph 2-2-3). The microprocessor in turn produces an inverted, non-overlapping clock signal (i.e., θ2) from the θ1 clock. The θ2 signal is present at pin 39 of UCD5. Two NOT gates, UB6A and UB6B, buffer the θ2 clock before it is sent to the VIAs (UCD4 and UAB1) and to the Write Logic. The θ2 signal is used to synchronize write operations, therefore the ROM does not require the θ2 signal.

The non-maskable interrupt ($\overline{NMI}$, UCD5, pin6) is disabled by R23 and is not used. The ready line (RDY, UCD5, pin 2) is held at a logic high by R22 and is also not used.

There are three lines entering the microprocessor which allow hardware devices in the VIC-1541 to change the sequence of instructions executed by UCD5. These lines are: Set Overflow (SO, pin 38), Interrupt ReQuest ($\overline{IRQ}$, pin 4) and ReSeT ($\overline{RST}$, pin 40). When the set overflow line goes high, it sets the overflow bit in the status register internal to UCD5. The sequence of instructions may be changed by testing the overflow (also known as carry) bit using the BCC (Branch if Carry Clear) or BCS (Branch if Carry Set) instructions.

When the interrupt request line goes low, the microprocessor calls the subroutine whose starting address is stored at locations $FFFE_{(H)}$ (LO byte) and $FFFF_{(H)}$ (HI byte). $FFFE_{(H)}$ contains $FE_{(H)}$ and $FFFF_{(H)}$ contains $67_{(H)}$. These two bytes form the 16 bit address $FE67_{(H)}$, which is the starting address of the interrupt routine. The $\overline{IRQ}$ line may be defeated or "masked" under software control.

When the $\overline{RST}$ line is pulled low, the microprocessor executes the instructions whose starting address is located at of $FFFD_{(H)}$ (HI byte) and $FFFC_{(H)}$ (LO byte). The address stored in these two locations is $EAA0_{(H)}$, which is the address of the first instruction of the reset routine. The reset routine initializes the VIC-1541.

2. ROM

UAB4 and UAB5 are 8K by 8 ROMs which together form a 16K ROM. The ROMs contain instructions which make up a machine language program called the DOS (Disk Operating System). The ROMs are located between addresses $C000_{(H)}$ and $FFFF_{(H)}$. Data is applied to the data bus (D0 thru D7) from the ROM when the $\overline{CE}$ line (pin 20) goes low. The address inputs (A0 thru A12) determine which one of the 8192 bytes in the ROM will be applied to the data bus. While the $\overline{CE}$ line is high, the data outputs are tri-stated and essentially disconnected from the data bus.

3. RAM

The RAM consists of four 1K by 4 RAM chips: UB3, UA3, UB2 and UA2. Together they form a 2K byte RAM. The RAM is located between addresses 0 ($0000_{(H)}$) and 2047 ($07FF_{(H)}$). Significant locations in RAM are:

0000-00FF	Zero Page
0100-01FF	Microprocessor Stack

The zero page contains variables, pointers and other data used by the DOS. The microprocessor stack is used for temporary storage of data.

When the MPU writes to the RAM, the data to be written is placed on the data bus (D0 thru D7), the location that the data is to be written into is placed on the address bus (A0 thru A15), and the $\overline{WR}$ (Write Enable) and $\overline{CS}$ (Chip Select) lines are brought low. When the MPU reads from the RAM, the location to be read is placed on the address bus (A0 thru A15) and the $\overline{CS}$ line is brought low. Data is then gated from the RAM to the data bus (D0 thru D7).

4. ADDRESS DECODER

The address decoder selects one of the following devices when the address bus contains an address within the address range of the device:

Device	Address range(Hex)
RAM,LO(UB2 & UA2)	0000-03FF
RAM,HI(UB3 & UA3)	0400-07FF
VIA,Serial Bus(UAB1)	1800-180F
VIA,Disk Control (UCD4)	1C00-1C0F
ROM,LO (UAB4)	C000-DFFF
ROM,HI (UAB5)	E000-FFFF

UB7B, UB7C and UB7D decode the ROM LO and ROM HI addresses. UB7C is configured as a NOT gate, which inverts A13 before it is applied to UB7D. UB7D enables UAB4, the LO ROM, when A15=logic 1 and A13=logic 0. UB7B enables UAB5, the HI ROM, when A15=logic 1 and A13=logic 1. A0 thru A12 are decoded by the selected HI or LO ROM. Notice that A14 is not decoded,

and therefore does not affect the operation of the decoder. The end result is two identical 16K blocks of ROM. Each of the ROM chips have two valid address ranges. One range is used with A14=logic 0 and the other range is used with A14=logic 1 as in the following table:

	A14=logic 0	A14=logic 1
ROM,LO(UAB4)	8000-9FFF	C000-DFFF
ROM,HI(UAB5)	A000-BFFF	E000-FFFF

Data which is read from address $8000_{(H)}$ is identical to the data read from address $C000_{(H)}$. This must be so because both addresses address the same location in the same ROM. The redundant 16K block between 8000 and BFFF is not normally used. It is just a by-product of the address decoder scheme. Notice that the read/write signals are not decoded for ROM addresses. The VIC-1541 hardware does not prevent a bus conflict between the microprocessor and the ROMs. The hardware design merely assumes any memory transfer at or above $8000_{(H)}$ is a read operation.

CAUTION

- NEVER WRITE TO MEMORY LOCATIONS AT OR ABOVE $8000_{(H)}$. A BUS CONFLICT MAY OCCUR, CAUSING PERMANENT DAMAGE TO UAB4, UAB5 or UCD5.

UB8, a BCD to decimal decoder, decodes the RAM and VIA address ranges. Address lines A10, A11 and A12 are connected to the A, B and C inputs, respectively, of UB8. As a result, the outputs of UB8 decode one of eight 1024 byte blocks. Address line A15 is applied to the D input of UB8. When the D input is a logic 0, one of the 0 thru 7 outputs will be active (i.e., logic 0). When the D input is a logic 1, outputs 0 thru 7 will be inactive, effectively disabling UB8. Any address at or below 7FFF will enable UB8. Any address at or above 8000 will enable the ROM array.

UB8, as noted previously, can decode one of eight 1024 byte blocks of memory. Notice that UB8 does not decode A13 or A14. As in the ROM adress decoder, this produces redundant images of the 8K block decoded by UB8. Since two bits are not decoded, UB8 produces four identical 8K blocks of memory as opposed to the two identical blocks produced by the ROM address decoder. The address ranges for each 8K block are as follows: 0000-1FFF, 2000-3FFF, 4000-5FFF, 6000-7FFF. Writing to location 0000 produces the same result as writing to locations 2000, 4000 or 6000. The redundant ranges of

2000-3FFF, 4000-5FFF and 6000-7FFF are not normally used.

The 0 output of UB8 is used to enable the low RAM pair (UB2 and UA2), while the 1 output is used to select the high RAM pair. The table below illustrates the RAM address range:

	Address ranges			
	A13=0,A14=0	A13=1,A14=0	A13=0,A14=1	A13=1,A14=1
RAM,LO	0000-03FF	2000-23FF	4000-43FF	6000-63FF
RAM,HI	0400-07FF	2400-27FF	4400-47FF	6400-64FF

The 2 thru 5 outputs of UB8 are not used. With four images being produced, this leaves the following locations not addressing any devices: 0800-17FF, 2800-37FF, 4800-57FF, 6800-77FF.

The 6 output of UB8 enables the serial bus VIA, UAB1. Notice that UAB1 decodes A0 thru A3. A4 thru A9 are not decoded, again producing redundant images. There are 64 images of the 16 VIA registers in the 1024 byte block enabled by UB8. There are also 4 images of each 1024 byte block that is selected. This gives a total of 256 images of the VIA registers. Typically the serial bus registers are accessed at $1800_{(H)}$-180F by the DOS.

The 7 output of UB8 is used to enable the disk controller VIA, UCD4. Again, this VIA has a total of 256 redundant images. Typically the disk controller VIA is accessed at $1C00_{(H)}$-1C0F by the DOS.

5. WRITE LOGIC

UB6C and UB7A form the write logic circuit. UB6C inverts the R/$\overline{W}$ (Read/$\overline{Write}$) line from pin 34 of UCD5. The output of UB6C will be high during a write cycle and will be applied to NAND gate UB7A together with the θ2 signal from UB6B. The output of UB7A drives the $\overline{WE}$ ($\overline{Write\ Enable}$) lines on the RAM chipsUB2, UB3,UA2 and UA3. The write logic for the VIAs is internal to the VIAs. Therefore the R/$\overline{W}$ line and the θ2 signal are applied directly to the VIA chips.

6. SERIAL BUS

The Serial Bus circuits consist of UAB1, UG2B, UD1, UC1A, UC1B, UC1E, UC1F and associated components. The Serial Bus circuits interface the computer with the Serial Bus and allow the VIC-1541 to communicate with the VIC-20/COMMODORE 64. The Serial Bus circuits also control the reset line for the VIC-1541 computer.

When power is first applied to the VIC-1541, C56 is in a discharged state, producing a logic 0 at the input of UD1E. This makes the output of UD1E a logic 1, which is applied to pin 9 of UD1D. The resulting logic 0 out of UD1D drives the reset line for UAB1, UCD4 and UCD5, causing them to assume their initialized states. After a short period of time, C56 will be charged thru R43 up to the logic threshold of UD1E. This causes the output of UD1E to change states. In turn, UD1D changes states and places the reset line high, allowing the computer to start execution of the DOS. If the VIC-20/COMMODORE 64 is reset, the reset line on the serial bus (pin 6 of P3 and P4) will go low (logic 0). This logic 0 is inverted by UC1E and applied as a logic 1 to the input of UD1F, which discharges C56 to a logic 0. Subsequent action of the reset circuit is as described above. CR17 is provided to discharge C56 if power is momentarily removed from the VIC-1541. The reset circuits are active only during power-up of the VIC-1541 or the VIC-20/COMMODORE 64.

The VIC-1541 serial bus is similar to the IEEE-488 bus (also known as GBIB or HPIB), but is slower and does not use some of the control signals. Like the IEEE-488 bus, the VIC-1541 bus may be interfaced with several peripherals, with each peripheral having a unique address. All the peripherals are daisy-chained together. Daisy-chaining means the first peripheral is connected to the computer, the second peeripheral is connected to the first, the third peripheral is connected to the second, etc. Daisy-chaining is the reason the two serial bus connectors, P3 and P4, are wired in parallel. The users of the bus (i.e., VIC-20/COMMODORE 64, VIC-1541, printers,etc) can be divided into three groups according to their activities at any given instant: controller, talker and listener.

Only the VIC-20/COMMODORE 64 may be a controller, talker and a listener. The peripherals may be either talkers or listeners. The controller dictates bus commands to the peripherals which tell the addressed device whether to talk, listen, untalk or unlisten. These bus commands are as follows:

Talk-Addresses a specific device and instructs the device to prepare to send data.

Untalk-Addressed device is instructed to cease transmissions.

Listen- Addressed device is instructed to prepare to receive data.

Unlisten-Addressed device is instructed to ignore any further data transmissions. Device will wait for next command.

The above bus commands are sent as an 8 bit byte. Five of the bits are used for the address and the others are used for the command definition. A total of 28 devices may be addressed by the serial bus. However, even though the address range of the serial bus is 4 thru 31, it can only drive 5 loads at any given time.

CAUTION

- CONNECTING MORE THAN 5 DEVICES TO THE SERIAL BUS COULD RESULT IN PERMANENT DAMAGE TO THE SERIAL BUS CIRCUITS.

Applicable bus signals used by the VIC-1541 are as follows:

SER CK-Primarily used to indicate that data is valid on the serial data line. Also used as a ready to send signal.

SER DATA-Primarily used to carry data bits. Also used as cleared to send, E01 acknowledge and handshaking signal.

SER ATN-When false, serial data contains data to be transferred. When active, indicates that the data bus contains a command. Only the controller may drive this line.

All of the above signals are active low signals. The signal lines are driven by open collector outputs, allowing all the peripherals to be WIRE-OR-ABLE. That is, any or all of the devices may drive the bus lines at the same time. If any device pulls a bus line active (low) the result will be an active line. In order for a line to be inactive (high), all peripherals must release the line to high.

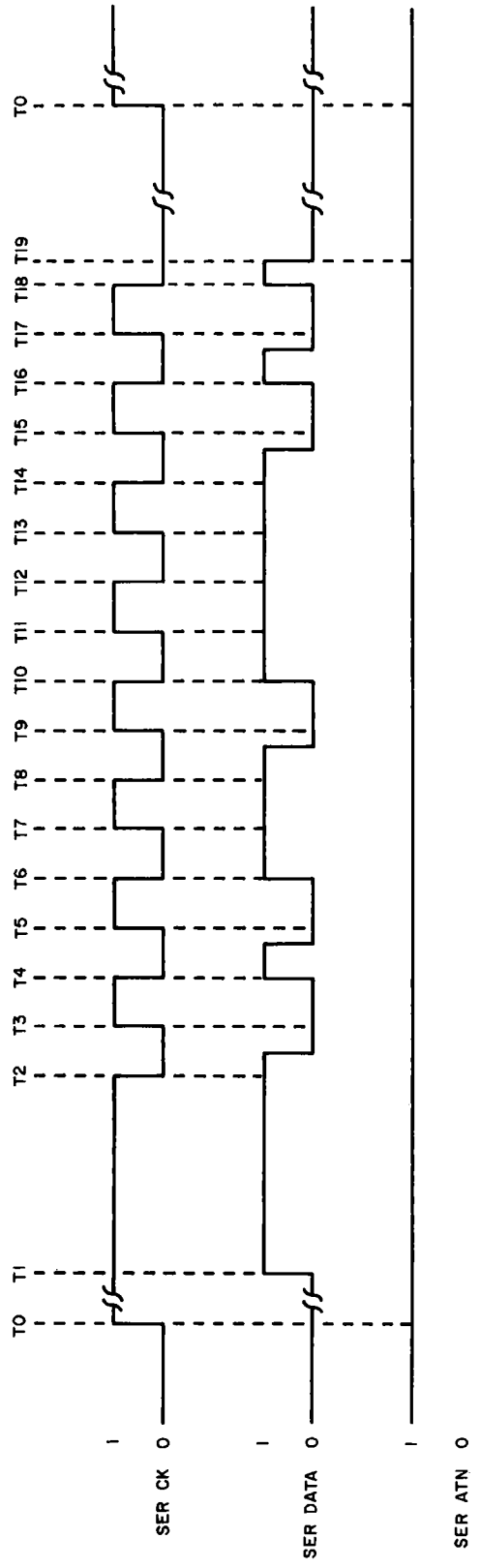


Figure 2-13 TYPICAL DATA TRANSMISSION

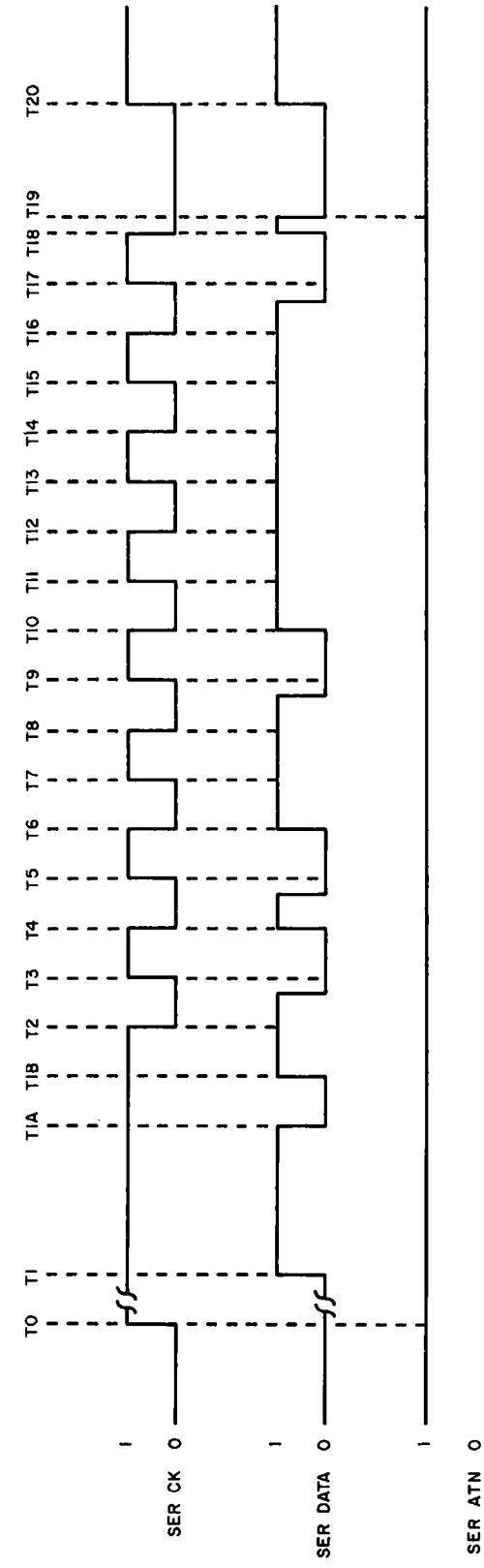


Figure 2-14 END OR IDENTIFY

Refer to Figure 2-13 for a typical data transmission signal. Prior to T0, the bus is in its standby state, the serial clock line is held low by the talker and the data line is held low by the listener. The SER ATN line is high, indicating the transmission to take place is data rather than a command. At T0, the talker signals ready to send by releasing the clock line. At T1, the listener acknowledges the ready to send by signaling clear to send. The listener signals clear to send by releasing the clock line to a logic high. If the listener is busy, it will not signal clear to send. The time between T0 and T1 is undefined and is determined by the listener. Within 200uS, the talker pulls the clock line low at T2. At some time between T2 and T3, the talker places the least significant bit on the SER DATA line. Since the bus lines are active low, the data appears inverted. That is, a low represents a true bit. At T3, the clock line is released to logic 1, indicating to the listener that the data bit on the SER DATA line is valid. The talker holds this condition until T4, where the talker releases the data line to a logic 1 and pulls the clock line low. This sequence continues until T18. After clocking in the most significant bit at T17, the talker once again pulls the clock line low and releases the data line at T18. Now the talker is waiting for the handshake signal which occurs at T19. At T19, the listener pulls the data line low. After T19, the serial bus is back in its standby condition, as it was prior to T0. Throughout the transmission of this byte, the talker keeps control of the clock line. The talker has control of the data bus from T2 to T18 only. The rest of the time the listener uses the data line for handshaking. Data transfers continue in this fashion until the last byte to be transferred. The last byte to be transferred contains "END OR IDENTIFY" handshaking.

The handshaking signal for "END OR IDENTIFY" takes place between T1 and T2 (Refer to Figure 2-14 for "END OR IDENTIFY" information). The talker signals "END OR IDENTIFY" by not pulling the clock line low for at least 200 uS. After approximately 200 uS, the listener acknowledges the "END OR IDENTIFY" at T1A by pulling the serial data line low. At T1B, the listener releases the SERIAL DATA line to logic 1, informing the talker to transmit the last byte. At T2, the talker pulls the clock line low and the byte is transmitted as previosly discussed. At some time after T19, the talker and the listener release the clock and data lines, respectively. These actions occur at T20.

A bus command is transmitted in the same manner as bus data , except that the SER ATN line is pulled low during the transmission. When a bus command is being transferred, the VIC-20/COMMODORE 64 is the bus controller and all the peripherals on the line become listeners. After the bus command, a secondary address may also appear. The secondary

address is optional and is used to control and specify a sub-channel. After the bus command is issued, the addressed device assumes the role issued by the bus command. Usually, the VIC-20/COMMODORE 64 assumes the opposite role. For example, if a talk command is issued the computer assumes the role of the listener. All the devices on the bus that are not involved with the transfer of data release control of the bus lines and await the next command (i.e., SER ATN pulled low). It is possible for the controller to issue a listen command to one peripheral and a talk command to another peripheral, causing data to be transferred between two peripherals while the VIC-20/COMMODORE 64 is free to perform other tasks. Such a possibility is difficult to accomplish, but the VIC-1541 bus is capable of doing so.

UC1F is the line receiver for the serial clock line. The output of UC1F is entered into the serial bus VIA, UAB1. When the VIC-1541 is a talker, it takes control of the serial clock line using port B, bit 3 (pin 13, UAB1) of the serial bus VIA. When pin 13 of UAB1 goes high, UD1C pulls the clock line active. UD1 has open collector outputs.

UC1A is the line receiver for the serial data line. The data is inverted and applied to the serial bus VIA. The serial data line is driven in the write mode by UD1A. The serial to parallel and parallel to serial conversions are performed by the software.

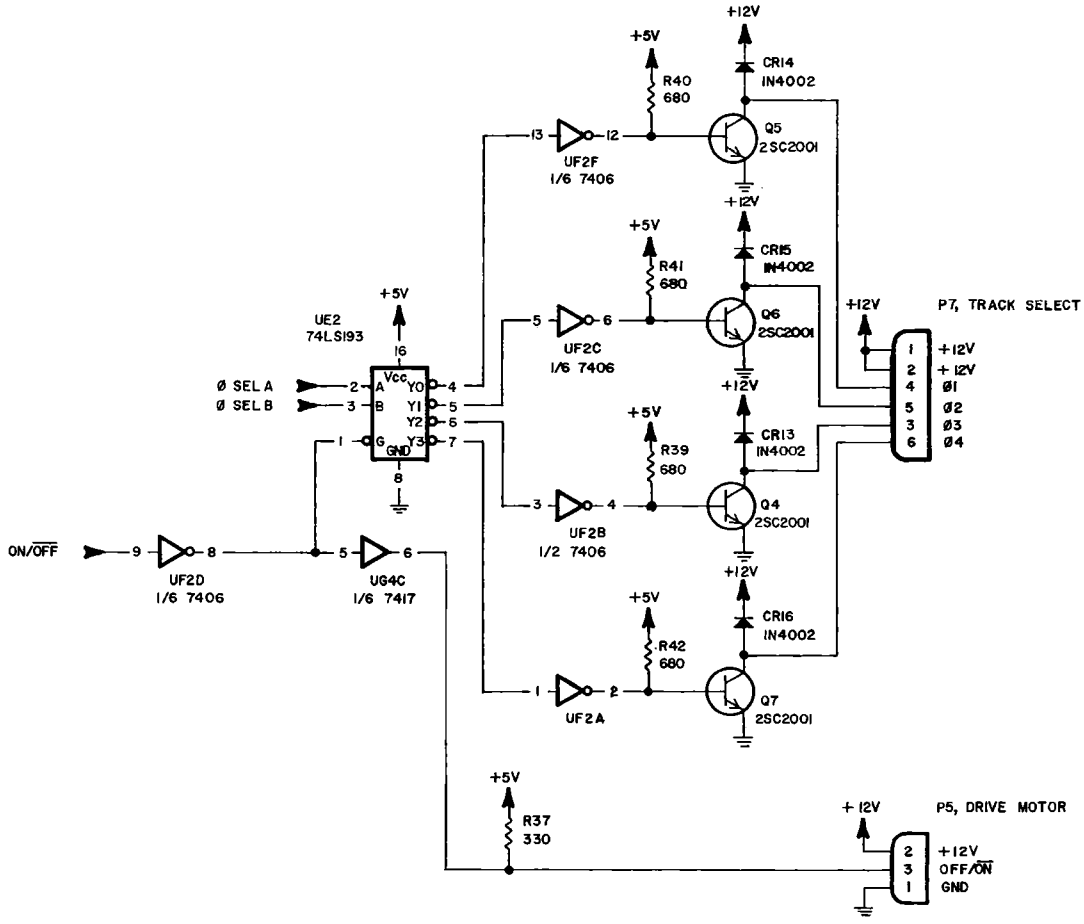
UC1B is the line receiver for the SER ATN line. The output of UC1B is applied to pin 40 of UAB1, generating an interrupt to the computer. The output is also applied to pin 17 to allow the computer to sample the state of the SER ATN line. When the SER ATN line is active, the serial data line is pulled low by UG2B and UD1B. The VIC-1541 releases the data line by using the other input (pin 4) of the Exclusive OR gate, UG2B.

E1 and E2 set the address of the VIC-1541. Refer to Section 3 for instructions on configuring E1 and E2.

UAB1 is a Versatile Interface Adapter (VIA) which contains two parallel ports, interrupt logic and two 16 bit counters, all of which are accessible to the computer through the data bus.

7. DISK CONTROLLER VIA

UCD4, the disk controller VIA, has two 8 bit ports which are used to interface with the Timing, Read, Write, Encoder/Decoder, Track Select and Optics circuits. UCD4 also contains interrupt logic and two 16 bit counters which may be accessed by the computer.



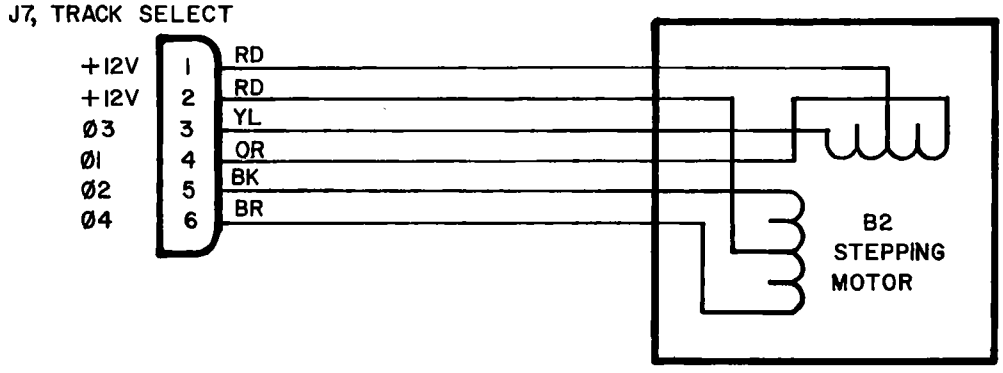


Figure 2-15. Track Select Circuit, Schematic.

2-3-5. **Track Select Electrical Theory** (Refer to Figures 2-15 and 2-16)

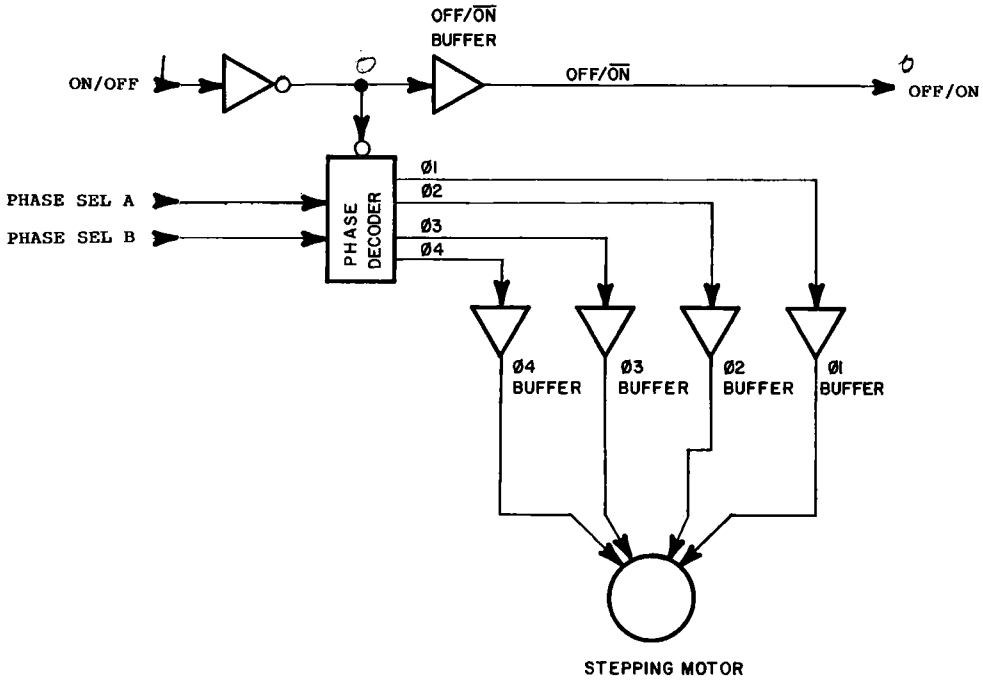


Figure 2-16. Track Select Circuit, Block Diagram.

The track select circuit consists of UE2, UF2A, UF2B, UF2C, UF2D, UF2F,UG4C and Q5 thru Q7. UE2, the phase decoder, pulls the selected θ(N) output low. To step inward (increasing track number), the four θ(N) lines must be clocked in ascending order (i.e., θ1,θ2,θ3,θ4,θ1,θ2...). To step outward the θ(N) lines must be clocked in descending order (i.e., θ4,θ3,θ2,θ1,θ4,θ3,...). Each of the θ(N) outputs is buffered by a NOT gate (UF2A,UF2B,UF2C,UF2F) and a transistor(Q5-Q7) configured as a common emitter buffer. The windings of B2 (the stepping motor) forms the collector loads for Q5-Q7. CR13-CR16 clip any overshoot produced by the inductive characteristics of the windings of B2 (the stepping motor).

When a logic 1 is applied to pin 9 of UF2D (ON/$\overline{\text{OFF}}$ line), the output of UE2 is enabled. When a logic 0 is applied to pin 9 of UF2D, the output of UE2 is disabled and none of the 0(N) lines are driven.

UG4C buffers the enable signal which enables UE2 and applies this signal to the motor driver servo circuit. Since the motor enable and step enable controls are both accomplished with the same line, tracks can only be changed while the drive motor (B1) is running. The following truth table illustrates the relationship between the ON/$\overline{\text{OFF}}$, θ SEL A and θ SEL B lines and the $\overline{\theta 1}$, $\overline{\theta 2}$, $\overline{\theta 3}$, $\overline{\theta 4}$ and OFF/$\overline{\text{ON}}$ lines.

ON/OFF	θ SEL A	θ SEL B	θ1	θ2	θ3	θ4	OFF/ON
0V	X	X	+12V	+12V	+12V	+12V	+5V
+5v	0V	0V	0V	+12V	+12V	+12V	0V
+5V	+5V	0V	+12V	0V	+12V	+12V	0V
+5V	0V	+5V	+12V	+12V	0V	+12V	0V
+5V	+5V	+5V	+12V	+12V	+12V	0V	0V

2-3-6. **Drive Motor System Electrical Theory** (Refer to Figures 2-17 and 2-18)

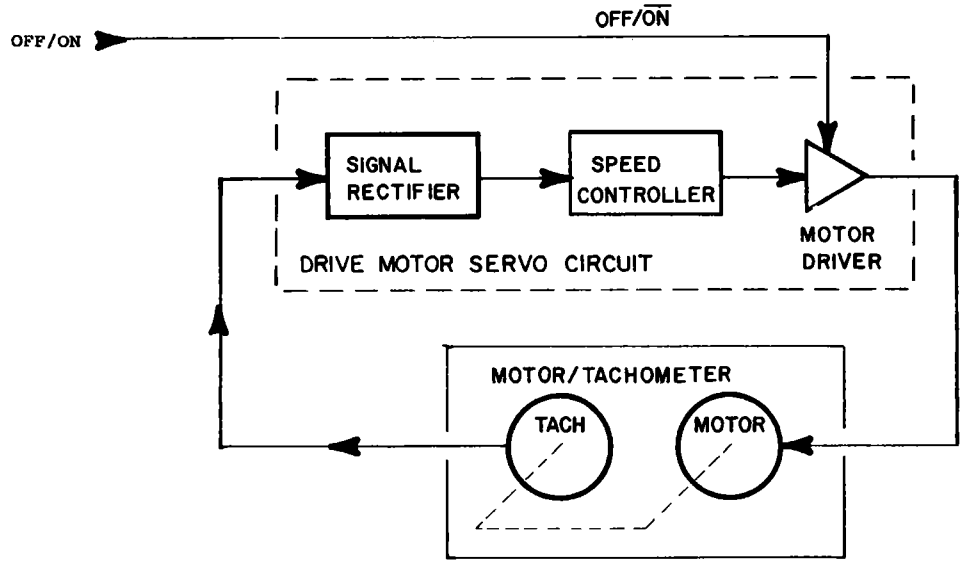


Figure 2-17. Drive Motor System, Block Diagram.

The purpose of the Drive Motor System is to maintain the disk at a constant speed. The drive motor system consists of the Drive Motor Servo circuit and the Drive Motor/Tachometer.

1. Drive Motor/Tachometer.

The Drive Motor/Tachometer contains a DC permanent magnet motor and a tachometer on a common shaft. The tachometer acts as a low power AC generator. The voltage output of the tachometer increases with increasing drive speed and provides feedback to the Drive Motor Servo circuit. This feedback contains motor speed information which the drive motor servo circuit uses to determine how hard to drive the motor. The Drive Motor Servo circuit adjusts the motor current as necessary to produce a specific speed as indicated by the tachometer feedback. This motor speed regulation is necessary since each floppy disk used in the drive may offer different mechanical loads to the motor. The drive motor system maintains the floppy disk at a constant speed of 300 RPM despite differences due to different manufacturers or age of the floppy disks.

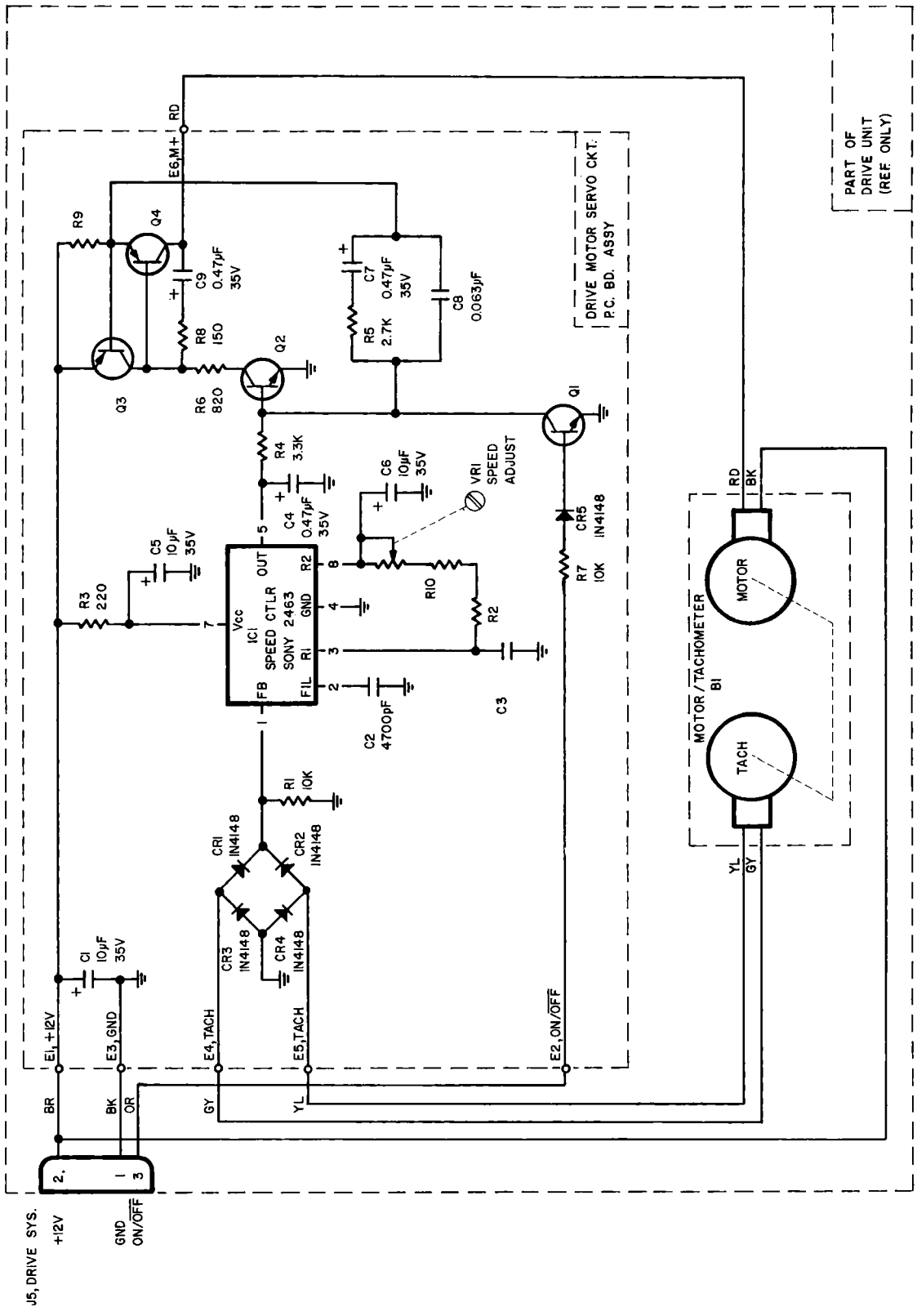


Figure 2-18. Drive Motor System, Schematic.

2. Drive Motor Servo Circuit.

Tachometer information enters the drive motor circuit at E4 and E5. This information, a sine wave, is rectified by the bridge rectifier consisting of CR1 thru CR4. R1 provides a load for the tachometer. The output of the rectifier is applied to pin 1 of IC1.

IC1 is the speed controller. Power is supplied through a lowpass filter (R3 and C5). C2 is also provided for filtering. R2, R10 and VR1 determine the speed of the floppy disk. VR1 is used to calibrate disk speed. C3 and C6 provide filtering. The output of IC1 (pin 5) will increase if the voltage at pin 1 is less than the threshold set by VR1. Conversely, the output at pin 5 will decrease if the voltage at pin 1 is greater than the voltage set by VR1. The circuit will settle when the feedback at pin 1 is equal to the threshold set by VR1. The output of the speed controller (IC1,pin 5) is applied to the motor driver.

The motor driver consists of Q1 thru Q4, R4 thru R9, C4 and C7 thru C9. Q2 is an inverting DC amplifier. C4 provides filtering. R4 limits base current. The combination of Q1, CR5 and R7 enables or disables the inverting DC amplifier, Q2. A logic low at E2 turns off Q1, allowing Q2 to operate normally. A logic high at E2 turns on Q1, shutting off Q2 by shunting its base current to ground, and thus shutting off the motor. Q4 is the final pass transistor. When its base is pulled low by Q2, through R6, it will conduct harder. As Q2 increases in conduction, Q4 will proportionately increase its own conduction. R9 and Q3 form a current limiter. As emitter current in Q4 increases, the voltage drop across R9 increases. When the drop across R9 reaches approximately 0.65 V, Q3 will conduct. When Q3 starts conducting, it shunts some of the bias current for Q4 to the positive supply. Q3 will shunt enough bias for Q4 to maintain motor current at a safe level for B1 (the Drive Motor). C7 thru C9, R5 and R8 control the slew rate and noise of the motor driver. The collector of Q4 is tied to the Drive Motor/Tachometer to complete the servo loop. C1 is provided to bypass noise from the +12 V supply.

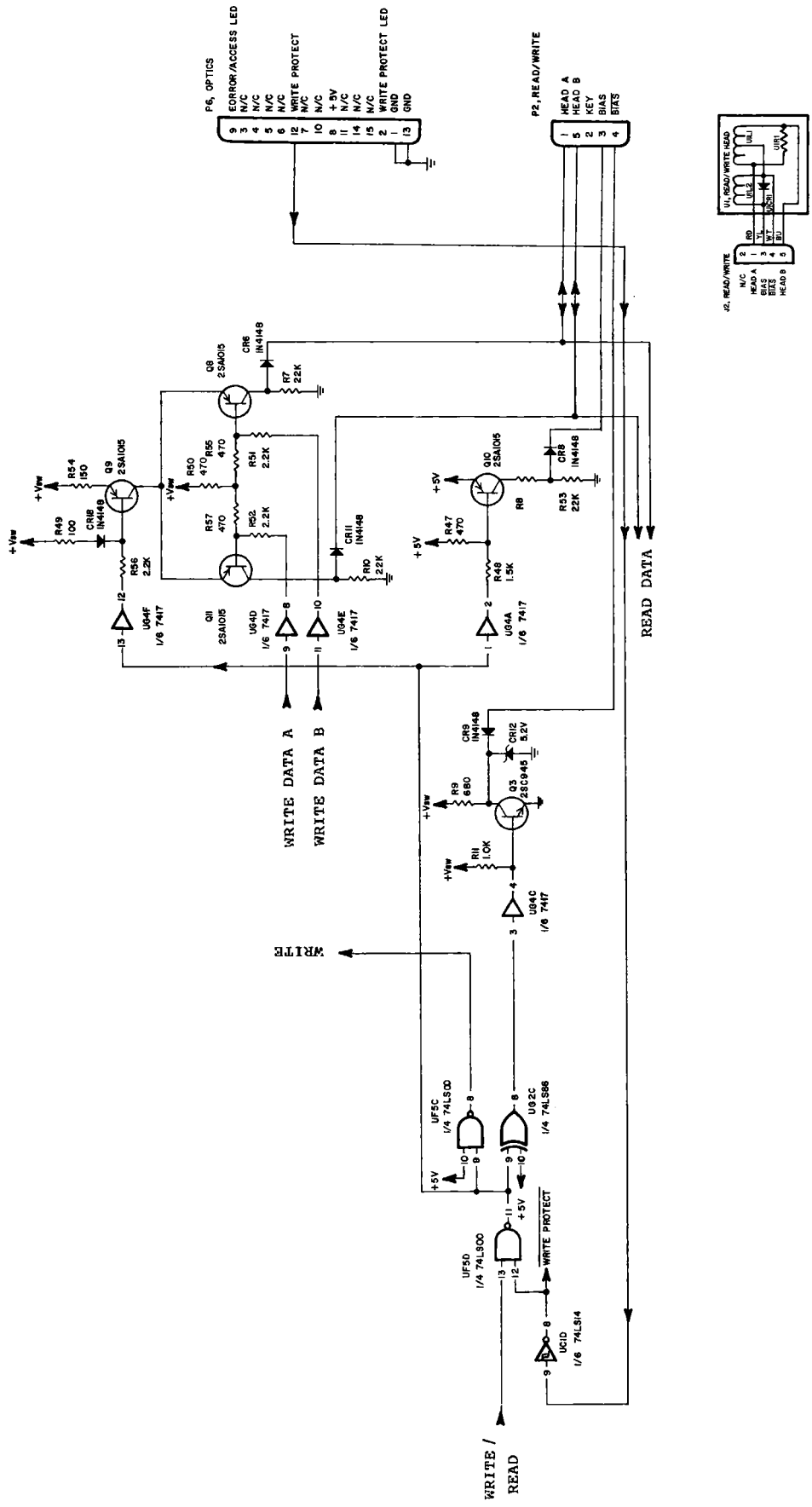


Figure 2-19. Write Circuit, Schematic.

2-3-7. **Write Circuit Electrical Theory** (Refer to Figures 2-19 and 2-20)

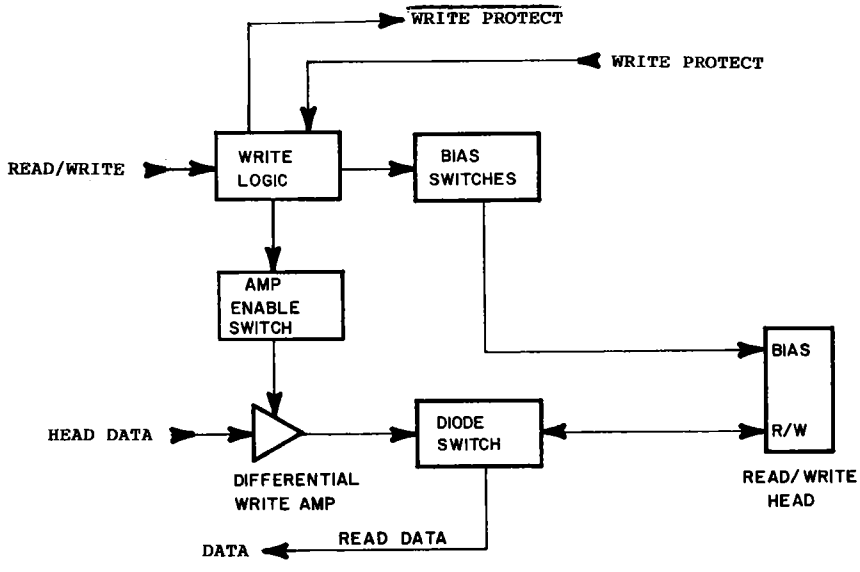


Figure 2-20. Write Circuit, Block Diagram.

The write circuit consists of the following major blocks: write logic, bias switch, amp enable switch, differential write amp and the diode switch.

1. Write Logic.

The write logic consists of UF5D, UF5A, UF5C, UG2C and UC1D. UC1D inverts the write protect signal and applies this signal to UF5D and to the disk controller VIA. When the output of UC1D is high, the write protect notch is uncovered. UF5A inverts the read/write line and applies its output to UF5D. The output of UF5D is active (active low) only if the write/read and WRITE PROTECT lines are both high. The output of UF5D is applied to the amp disable switch, one of the bias switches, to UF5C (a NAND gate configured as an inverter) and to UG2C (an EXCLUSIVE OR gate also configured as an inverter). The output of UF5C (which is high when writing) is applied to pins 13 and 10 of UF6B, which in turn enables the flip-flop. The output of UG2C is applied to the bias switch.

2. Bias Switch.

During a write operation, the bias switch applies current through the bias winding (U1L2) in the read/write head. One

side of the bias switch, Q10, drives the positive side of the bias winding. Q10 is gaited into conduction by the input of UG4A, which is low when writing. The other side of the bias switch, Q3, drives the negative side of the bias winding. Q3 is driven into conduction by the input of UG4C, which is high when writing. Bias current flows through U1L2 via Q10, R8, Q3, CR8 and CR9 (both diodes are forward biased).

3. Amp Enable Switch.

The amp enable switch consists of Q9 and UG4F. A low is applied to UG4F while writing, driving Q9 into conduction. When Q9 is conducting, power is applied to the differential write amp.

4. Differential Write Amp.

The differential write amp consists of UG4D, UG4E, Q8 and Q11. UG4D and UG4E are driven by the Encoder/Decoder and in turn drive the differential transistor pair, Q8 and Q11. When Q8 is conducting, Q11 is turned off. When Q11 is conducting, Q8 is turned off. The outputs of the differental write amp are applied to the read/write head via the diode switch.

5. Diode Switch.

The diode switch consists of CR6 and CR11. When in the write mode, the center tap of the read/write winding (U1L1) is at ground potential because of bias switch Q3 and CR9. When Q3 goes into conduction, current flows through the read/write winding via either Q11, CR11, CR9 and Q3 or via Q8, CR6, CR9 and Q3, depending upon the state of the differential write data from the Encoder/Decoder circuit.

2-3-8. **Read Circuit Electrical Theory** (Refer to Figures 2-21 and 2-22)

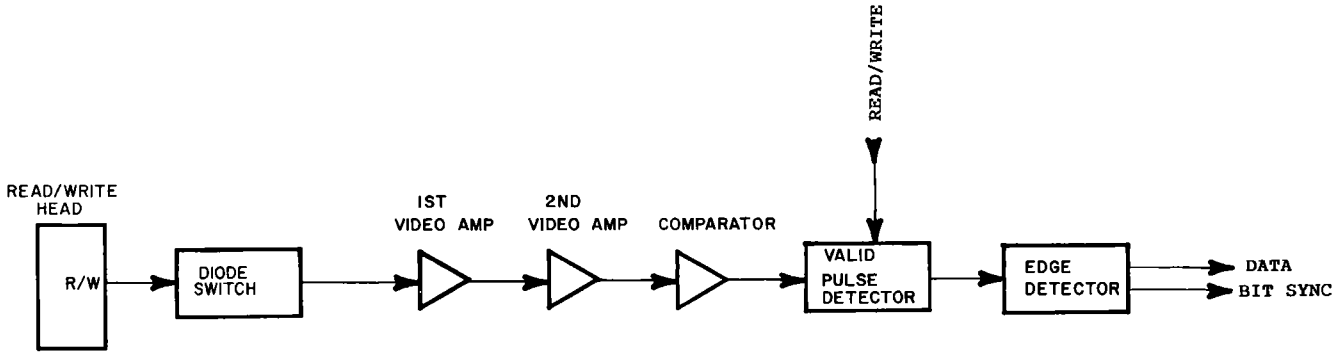


Figure 2-21. Read Circuit, Block Diagram.

The read circuit senses and amplifies data from the floppy disk. The amplified data is checked for valid pulse widths to improve noise immunity. The output of the read circuit is a narrow pulse which occurs on both the rising and falling edges of the data.

The read circuit does not care if the data is high or low. Only the positions of the transitions are significant. The data is divided into clock cells and bit cells. Clock cells are located just prior to a bit cell. If a transition occurs at the beginning of a cell, the cell is interpreted as a logic 1. If no transition occurred, the cell is interpreted as a logic 0.

The data is sensed by the read/write head and applied to the first video amplifier (UH7) via the diode switch (Refer to Figure 2-21). When in the read mode, Q9, Q10 and Q3 are not *conducting. CR7 and CR10 are forward biased via R12, R13,* U1L1, CR9 (which is also forward biased) and CR12 (a 5.2 V Zener diode). The cathodes of CR7 and CR10 are at approximately +6 V, causing the data to be applied to the first video amplifier (UH7). The +6 V bias is applied to the cathodes of CR11 and CR6.

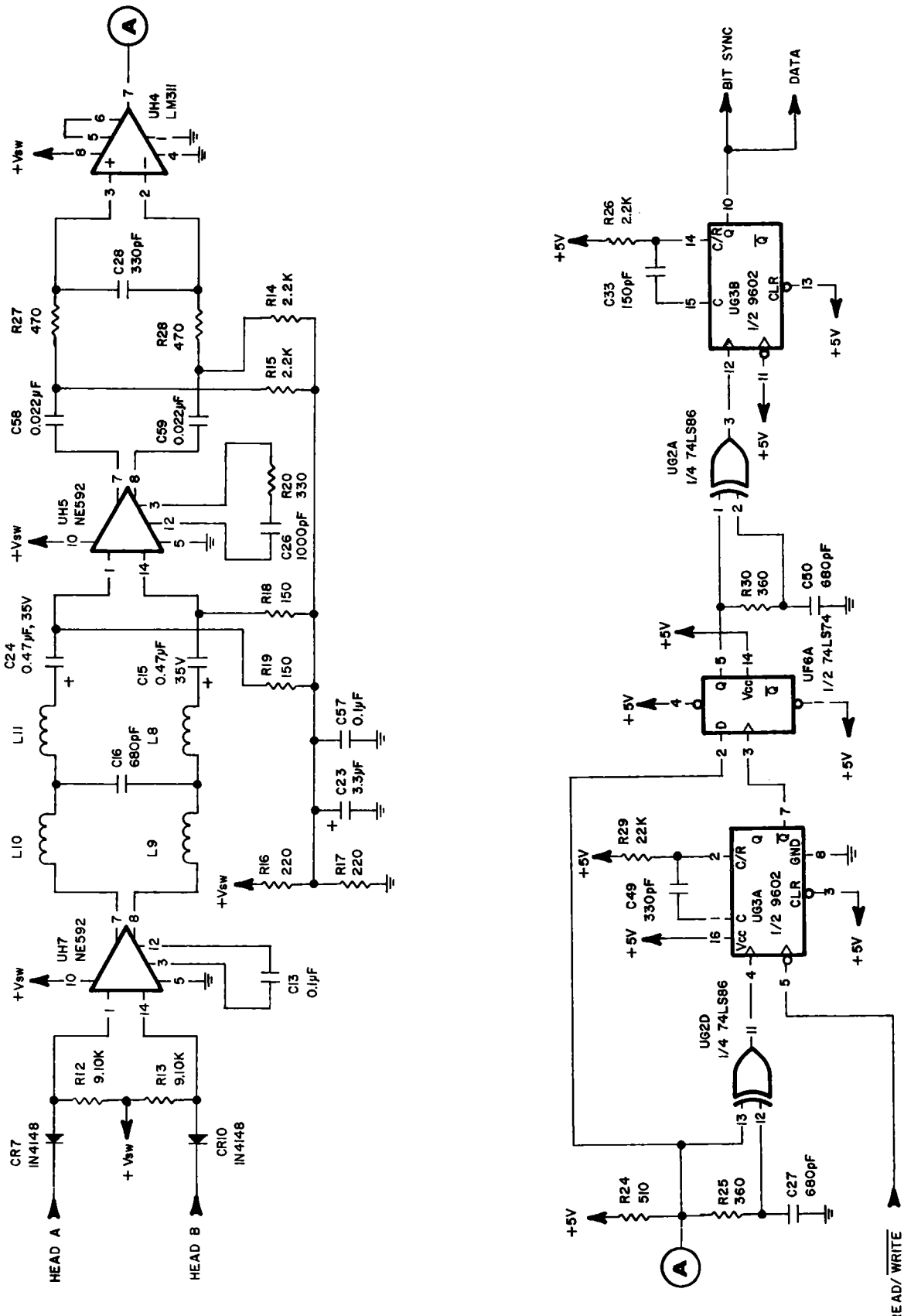


Figure 2-22. Read Circuit, Schematic.

Since Q9 is not conducting, R10 and R7 pull the anodes of CR11 and CR6 to ground, causing CR11 and CR6 to be reverse biased and isolating the write circuit from the read circuit. CR8 is also reverse biased, since the +6 V bias on the cathodes of CR7 and CR11 is applied to the cathode of CR8 via the read/write winding (U1L1) and the bias winding (U1L2).

(Refer to Figure 2-22.) The output of UH7, the first video amplifier, is applied to a lowpass filter formed by L8 thru L11 and C16. C15 and C24 block the DC offset out of UH7 to prevent the offset from disturbing the input bias to UH5. R16 and R17 set a bias voltage of +6 V, which is filtered by C23 and C57 and applied to the input signal of UH5 via R18 and R19. The output of UH5 is applied to the comparator via C58, C59, R27 and R28. C58 and C59 block the DC offset out of UH5 to prevent the offset from affecting the bias on the input of the comparator,UH4. A +6 V bias is applied to the input signal of the comparator from R16 and R17 via R14 and R15.

The output of the comparator is applied to the valid pulse detector (UG2D, UG3A and UF6A). UG2D, along with C27, R24 and R25, forms an edge detector. Pin 11 of UG2D will produce a 500 nS active high pulse on rising edges of the comparators' output and will produce a 150 nS active high pulse on falling edges of the comparators' output. The pulse out of UG2D is applied to UG3A, a single-shot multivibrator. UG3A produces an active low pulse which is approximately 2.5 microseconds wide. Flip-flop UF6A is clocked on the trailing edge of the output pulse of UG3A. The output of the comparator must be maintained for at least 2.5 microseconds in order to be latched into the flip-flop. If a narrow noise pulse triggers this circuit, the output of the flip-flop will not change since the noise pulse will terminate before UG3A triggers UF6A. The output of the fli-flop (UF6A) will reflect the data delayed by approximately 2.5 microseconds.

The valid data out of the valid pulse detector is applied to an edge detector consisting of UG2A and UG3B. UG2A operates the same as UG2D in the previous paragraph. The pulses out of UG2A trigger UG3B, a single-shot multivibrator. UG3B produces a narrow pulse which represents transitions of the data. This output is applied to the timing circuit to synchronize the ENCODER/DECODER Clock, and to the Encoder/Decoder which will detect the data and perform a serial to parallel conversion. Notice that pin 5 of UG3A is connected to the READ/$\overline{\text{WRITE}}$ line, causing the valid pulse detector to be disabled during a write operation.

The video amplifiers will often oscillate with no data in, but these oscillations are high enough in frequency that they seldom get past the valid pulse detector.

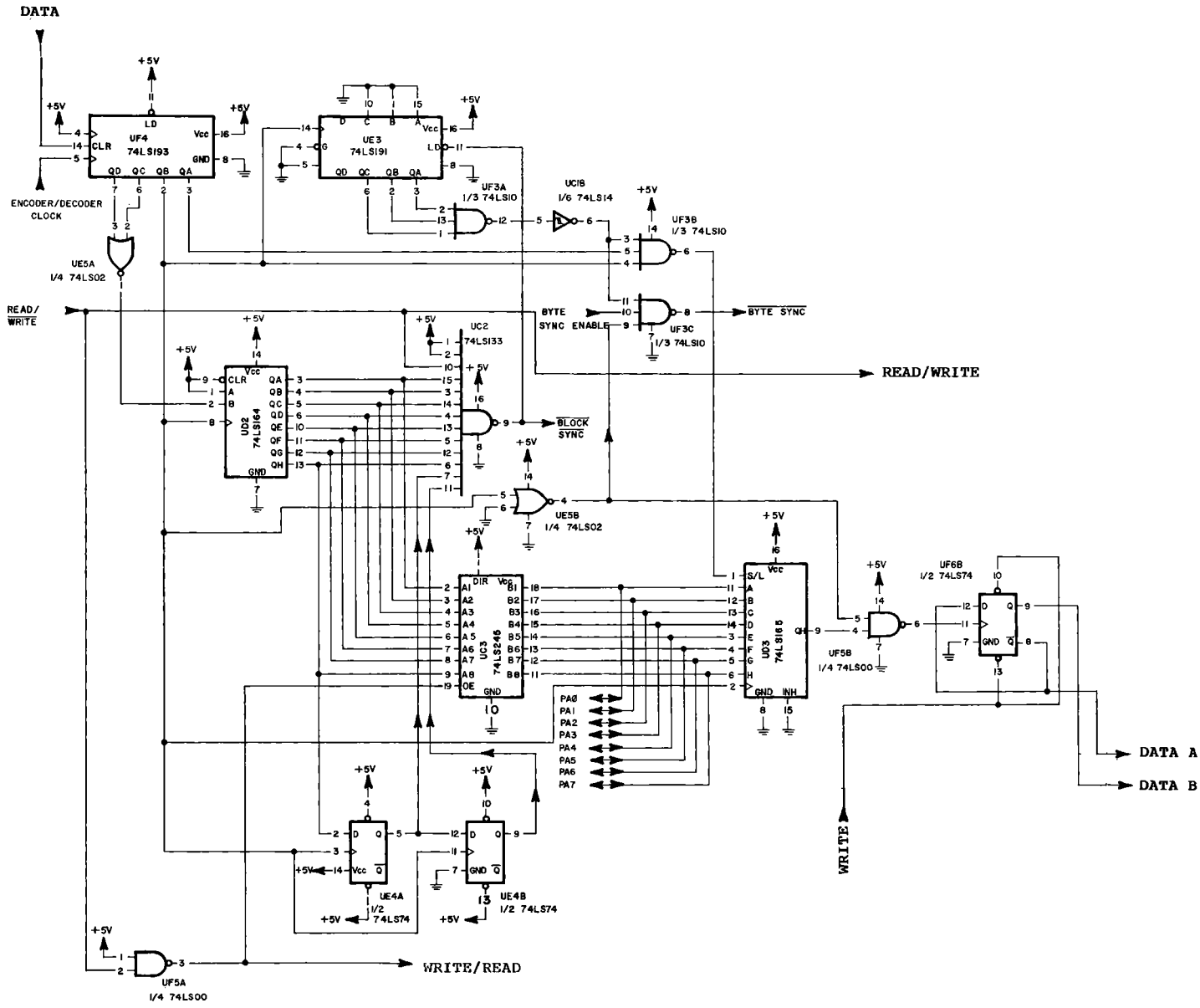


Figure 2-23. Encoder/Decoder Circuit, Schematic.

2-3-9. **Encoder/Decoder Electrical Theory** (Refer to Figures 2-23 and 2-24)

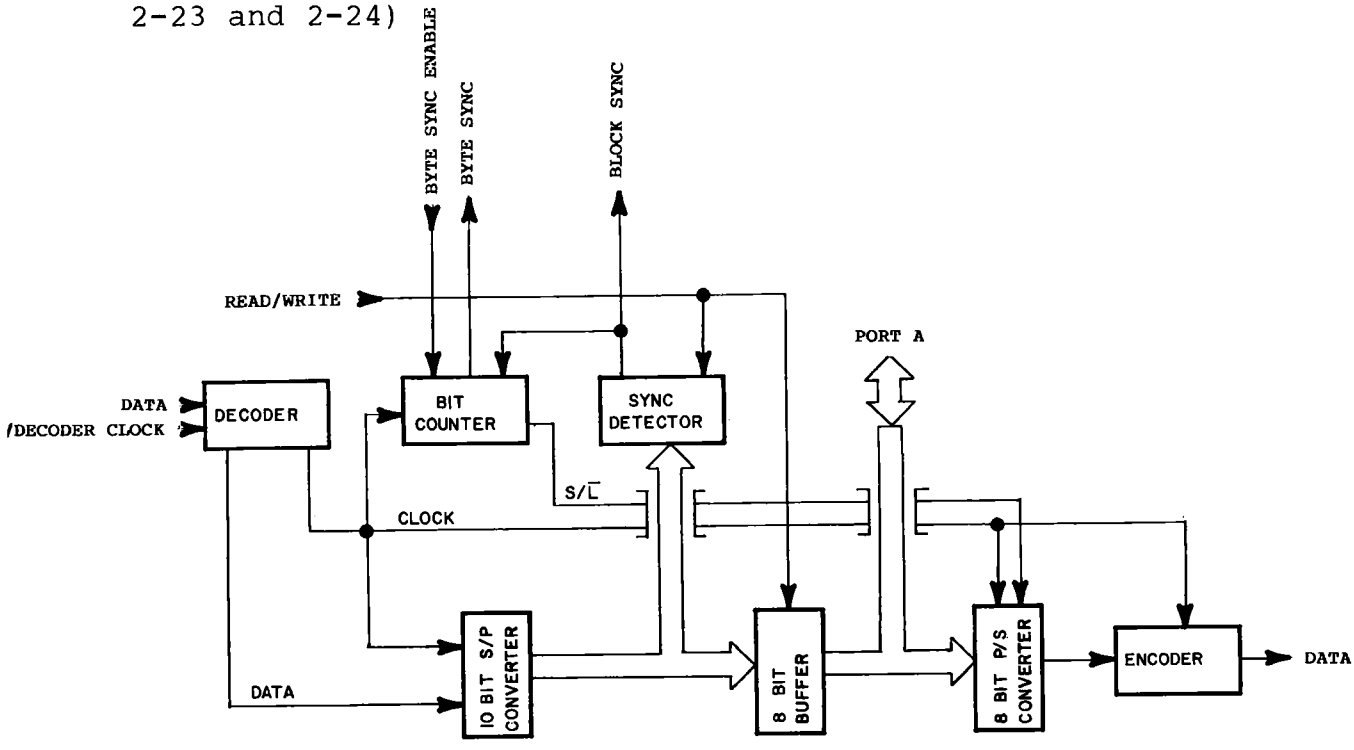


Figure 2-24. Encoder/Decoder Circuit, Block Diagram.

The Encoder/Decoder circuit encodes and decodes the transition positions which are written to, or read off of, the disk. The encoder/decoder circuit also performs the serial to parallel and parallel to serial conversions necessary to move the data between the computer and the floppy disk.

1. Decoder.

The decoder consists of UF4 and UE5A. The decoder has two outputs. Pin 1 of UE5A is the serial data output and pin 2 of UF4 is the serial clock output. The serial data output contains a clock bit in between data bits. The serial clock output is high whenever clock or data bits are valid on the serial data line.

A bit/clock cell is four ENCODER/DECODER clock pulses wide. As mentioned in Read Circuit Theory, if a transition (or pulse into the decoder) occurs at the beginning of a bit/clock cell, that cell is a logic 1. If no transition occurs, the cell is a logic 0. When a transition does occur, UF4 (a binary counter) is cleared and the timing circuit is reset to start the ENCODER/DECODER clock at the beginning of its cycle. Pins 6 and 7 of UF4 are at logic lows, causing the output of UE5A, the serial data line, to go to a logic 1.

Two ENCODER/DECODER clock pulses later, the serial clock (pin 2 of UF4) goes high. When the serial clock line is high, the serial data line is valid. The serial clock line remains high for two clock cycles.

A bit cell is now complete. At this time, pins 2 and 3 of UF4 will again be logic 0 and pin 6 will be a logic 1. The logic 1 on pin 6 of UF4 causes the serial data line (pin 1 of UE5A) to be a logic 0. If no transition occurs at the beginning of the next bit/clock cell, the serial data line will remain at a logic 0 when the serial clock line goes high two ENCODER/DECODER clock cycles into the bit/clock cell.

2. Bit Counter.

The bit counter produces the $\overline{\text{BYTE SYNC}}$ signal to the microprocessor and the shift/load signal for the parallel to serial converter. UE3, UF3 and UC1B form the bit counter. UE3 is a four bit binary counter which is clocked by the serial clock. Every eight serial clock pulses, when the outputs of QA, QB and QC go to logic 1, the output of UF3A goes low. The logic 0 from UF3A causes the output of UC1B to go high. The high output of UC1B is then applied to UF3B and UF3G. UF3C NANDs the output of UC1B with the byte sync enable line from the disk controller VIA and with the inverted serial clock from UE5B. The output of UF3C informs the microprocessor that a byte is ready to be read into the computer. When in the write mode, the output of UF3C is used to indicate that the next byte to be written should be loaded.

UF3B NANDS the output of UC1B with the serial clock and with the QA output of UF4. The output of UF3B, when low, causes the next byte to be transmitted to be loaded into the parallel to serial converter.

3. Serial to Parallel Converter.

The serial to parallel converter consists of UD2 and UE4. UD2 produces eight bits in parallel which may be entered into the computer. UE4 adds an additional two bits, which are used to detect block sync signals. Serial data is presented to the input of UD2 (pin 2). The serial clock, which is applied to the clock input of UD2 (pin 8), shifts the contents of the serial to parallel converter on its rising edge. Every other bit present on the output of the serial to parallel converter is a clock bit. The computer removes these clock bits and constructs a nibble from the eight bits present at the output of the serial to parallel converter. The computer must read two bytes of data from the Encoder/Decoder in order to construct one byte of data from the disk.

4. Buffer.

The buffer, UC3, gates data onto port A of UCD4 when in the read mode. When in the write mode, the buffer is tri-stated, allowing data from port A of UCD4 to be applied to the parallel to serial converter without conflict from UD2.

5. Sync Detector.

A block sync signal consists of at least 16 logic 1's (clock and data bits set to logic 1). During a read operation the output of UC2 goes low when 10 consecutive logic 1's are detected by the serial to parallel converter. The block sync signal is available on pin 9 of UC2. The leading edge of the block sync signal interrupts the computer, which then monitors the signal until its falling edge. After the falling edge occurs, the computer enables the byte sync and waits for the byte sync to become active. When the byte sync becomes active, the received byte is loaded into the computer. All received data is synchronized in this manner.

6. Parallel to Serial Converter.

In the write mode, data from port A of UCD5 is applied to the parallel to serial converter, UD3. When the output of UF3B becomes active, the byte to be written is loaded into the serial to parallel converter. The inverted clock signal is used to shift bits out of the parallel to serial converter. UF3C informs the computer to load the next byte which is to be written.

7. Encoder.

The encoder consists of UF5B and UF6B. The encoder must produce a transition for each high bit presented to it and must not produce a transition for a low bit. UF5B gates the inverted clock signal to the flip-flop (UF6B) when a high is applied to UF5B from UD3. When a low from UD3 is applied to UF5B, no clock pulse is gaited to UF6B. UF6B will change states whenever a clock pulse is applied to pin 11. The result is a transition for every high bit out of UD3. UF6B may be disabled by applying a logic low to pins 13 and 12 of UF6B. The complementary outputs of UF6B are available on pins 8 and 9 and are applied to the Write circuit

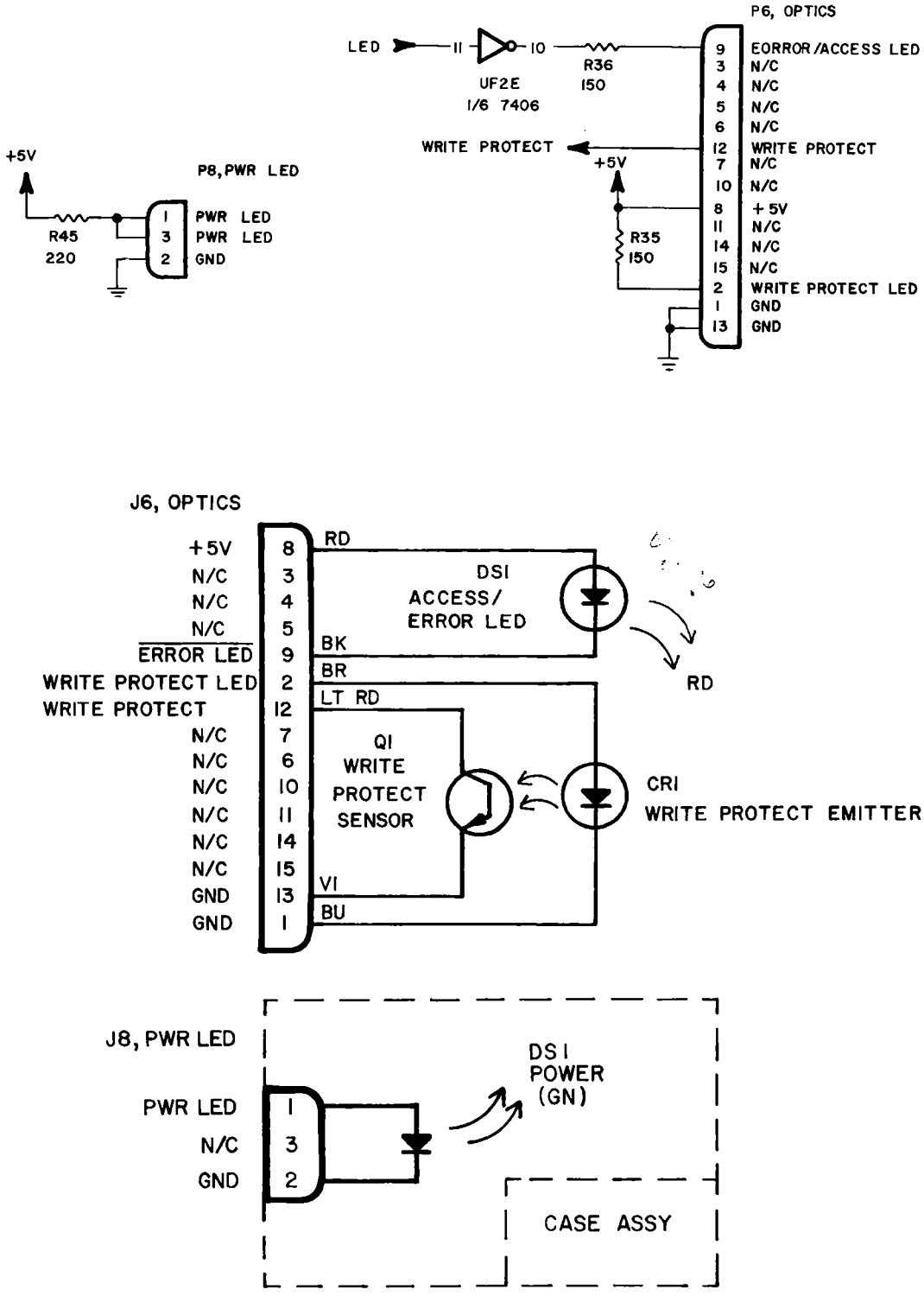


Figure 2-25. Optics Circuit, Schematic.

2-3-10. **Optics Circuit Electrical Theory** (Refer to Figures 2-25 and 2-26)

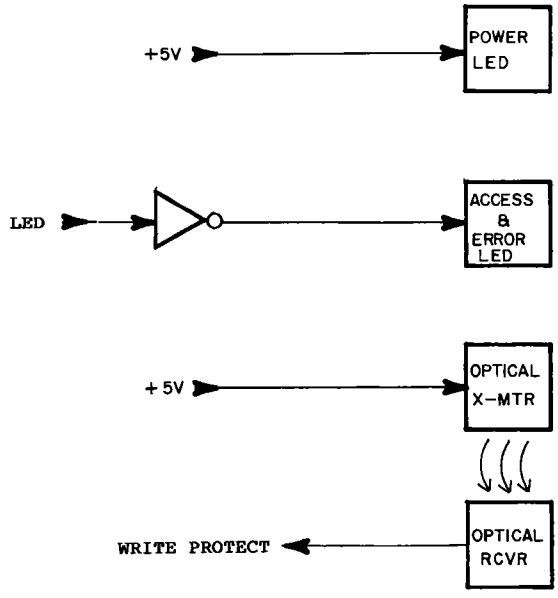


Figure 2-26. Optics Circuit, Block Diagram.

The optics circuits consist of: DS1 on the case assembly; DS1, CR1 and Q1 on the drive unit; and UF2E, R35, R36 and R54 on the disk controller PC Board.

R45 provides current limiting for the Power LED, DS1 on the case assembly. R35 provides current limiting for CR1, the optical transmitter, on the drive unit. Both CR1 on the drive unit and DS1 on the case assembly come on as soon as the +5V line becomes active (Power On). The optical receiver, Q1 on the drive unit, is positioned under CR1 in such a manner that the write protect notch is directly between them when the floppy disk is seated. Q1 on the drive unit conducts (produces a logic 0) when the write protect notch is left uncovered (writing permitted). When the write protect notch is covered, Q1 on the drive unit is not conducting (logic 1). The write protect output of the optical receiver is available on pin 12 of P6 and is applied to the Write circuit.

UF2E drives the Access/Error LED. A high on the LED line causes DS1 on the drive unit to illuminate. R36 limits the current through DS1.

SECTION 3
INITIAL CONFIGURATION

Section 3-INITIAL CONFIGURATION

3-1. General

This section provides step-by step procedures for setting the AC line voltage (selectable between 115 VAC and 230 VAC) and the device number (selectable between 8,9,10 or 11).

3-2. AC Power

The VIC-1541 may be configured for 115 VAC at 50-60 Hz, or for 230 VAC at 50-60 Hz. To change power configuration, perform the following steps:

1. Disconnect AC power cord from J9.

2. Disconnect serial bus cable(s) from J3 and/or J4.

3. Remove top cover. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

4. Remove RFI shield. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

5. Remove Disk Controller P.C. Board. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

6. Desolder wire from pin 1 of J9. (Refer to Figure 3-1)

7. Solder desired tap of T1 to pin 1 of J9:

   a. Solder black tap of T1 to pin 1 of J9 for 115 VAC operation. (Refer to Frame Schematic)

   b. Solder red tap of T1 to pin 1 of J9 for 230 VAC operation. (Refer to Frame Schematic)

WARNING

- TO PREVENT A POSSIBLE SAFETY HAZARD, INSULATE PIN 1 OF T1 WITH HEAT SHRINK TUBING OR EQUIVALENT. USING HEAT SHRINK OR ELECTRICAL TAPE, INSULATE UNUSED TAP OF T1 AS SHOWN IN FIGURE 3-1.

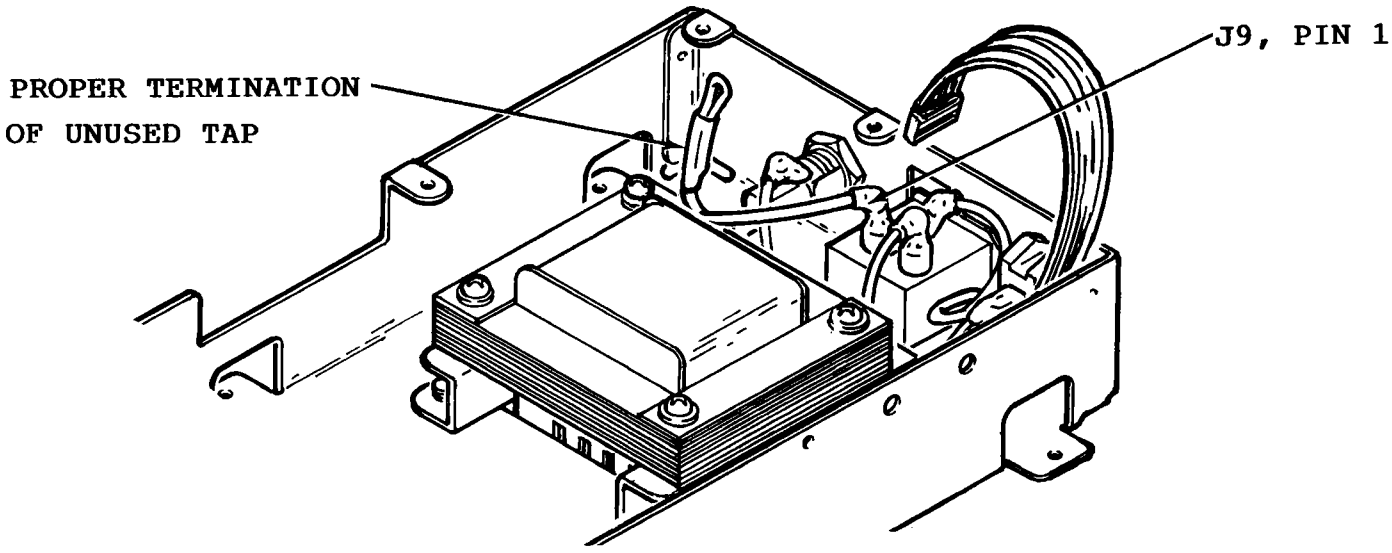


Figure 3-1. Electrical insulation of unused tap and pin 1 of J9.

WARNING

DO NOT CAP OFF UNUSED TAP OF T1 AS SHOWN IN FIGURE 3-2. SUCH A METHOD MAY CREATE A SAFETY HAZARD IN TIME.

8. Reassemble the VIC-1541. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

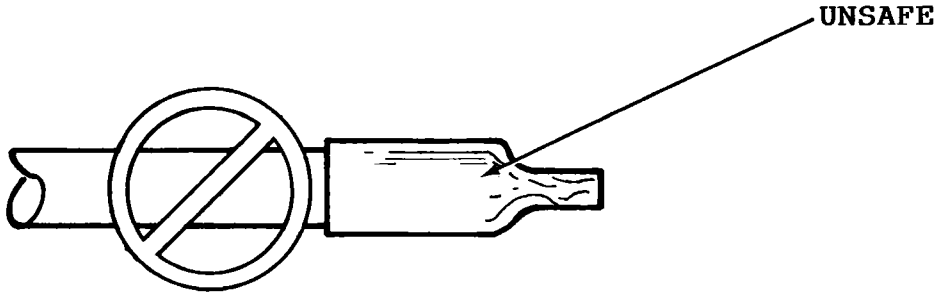


Figure 3-2. Example of unsafe insulation of unused tap.

3-3. **Device Number.**

The VIC-1541 is factory-configured for device #8. If more than one VIC-1541 is to be connected to the serial bus, the additional drive(s) will require a different device number(s).

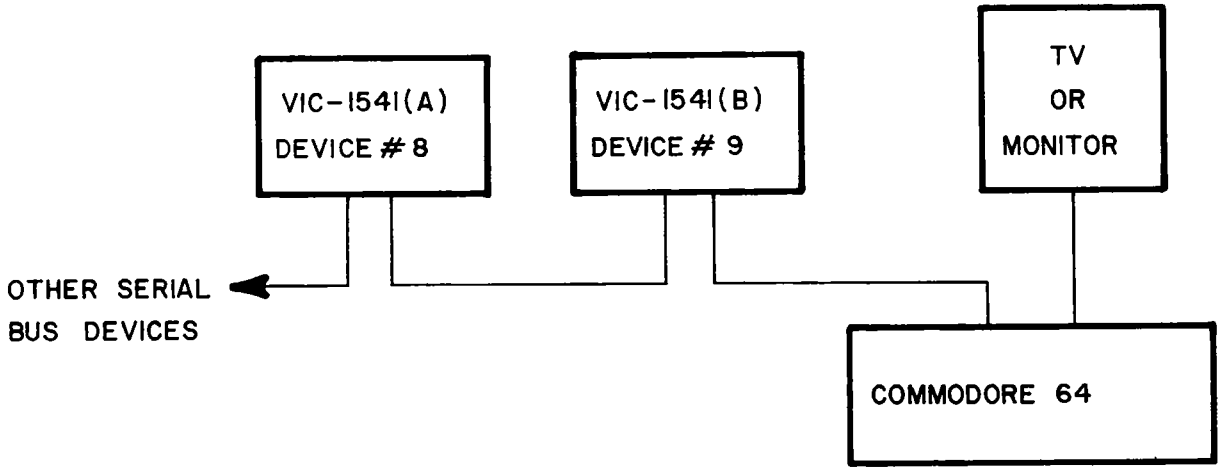


Figure 3-3. Multiple Disk Drive Configuration

Figure 3-3 illustrates a system with two VIC-1541's on line at the same time. VIC-1541 (A) is configured for device #8 and VIC-1541 (B) is configured for device #9. To illustrate the difference in commands required for two or more disk drives, assume that each drive contains a blank disc that is to be formatted. To format the disk in drive (A), the following command in Figure 3-4 could be used:

```
OPEN 15,8,15,"N0:EXAMPLE,01"<Return>
     |  |  |
     |  |  +-- Channel #
     |  +----- Device #
     +-------- Logical file #
```

Figure 3-4. Format Command, Drive A

To format the disk in drive (B), the following command in Figure 3-5 could be used:

```
OPEN 16,9,15,"N0:EXAMPLE,01"<Return>
     |  |  |
     |  |  +-- Channel #
     |  +----- Device #
     +-------- Logical file #
```

Figure 3-5. Format Command, Drive B

Notice that the device # and logical file # change. Device #9 in the second command addresses VIC-1541 (B). The logical file # in the second command has changed because logical file #15 is aready opened and assigned to device #8 in the first command. If logical

file #15 were closed between the first and second commands, the second command could have used logical file #15 instead of logical file #16.

The VIC-1541 may be configured as device #8,9,10 or 11. To change device numbers proceed as follows:

NOTE

- At least one VIC-1541 should be configured as device #8 since most pre-packaged software assumes that the disk drive is device #8.

1. Disconnect AC power cord from J9.

2. Disconnect serial bus cable(s) from P3 and/or P4.

3. Remove top cover. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

3. Remove RFI shield. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

4. Locate the device # programming pads next to UAB1 and P5. (Refer to Figure 3-6.)

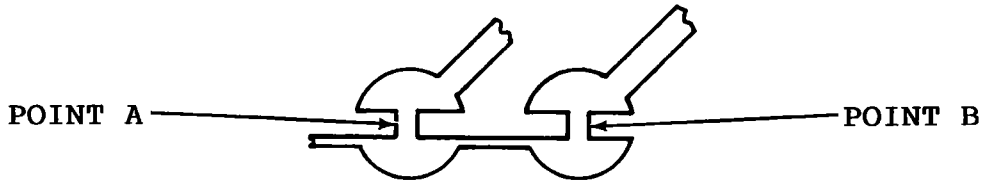


Figure 3-6. Device # programming pads

5. Points A and/or B may be cut to change device number. Use the following table to determine which points (A and/or B) to cut:

Device #	Point A	Point B
8	not cut	not cut
9	cut	not cut
10	not cut	cut
11	cut	cut

NOTE

- If a path has previously been cut and is now desired to be "not cut", solder a short bare wire between the pads. (Refer to Figure 3-7)

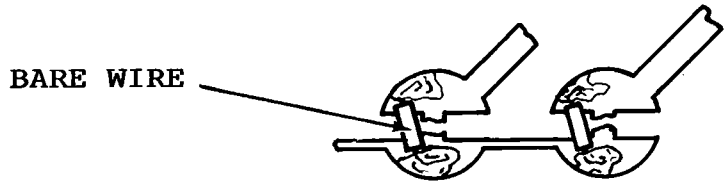


Figure 3-7. Reconfiguration of Device #

6. Reassemble the VIC-1541. (Refer to Section6-DISASSEMBLY/REASSEMBLY)

SECTION 4
PERFORMANCE TEST

NOTE

- If the VIC-1541 being tested has been assigned a device number other than 8 (Refer to Section 3-INITIAL CONFIGURATION), the performance test program must be modified. Modify the program by changing all device number references in the "open" statements from 8 to the device number of the VIC-1541 being tested.

4. Run the performance test program. Verify disk passes test.

NOTE

- Ensure that the write protect notch on the blank disk is left uncovered.

5. Cover write protect notch on blank disk with opaque tape.

6. Run performance test again. Verify disk drive does not pass test.

7. Remove floppy disk from disk drive.

8. Enter following command into VIC-20/COMMODORE 64:

LOAD"$",8 <Return>

NOTE

- If device number of the disk drive being tested is other than 8, replace the 8 in the above command with the correct device number.

9. Verify that the red LED on the front of the VIC-1541 is flashing.

SECTION 5
CALIBRATION

Section 5-CALIBRATION

5-1. General

This section contains step-by-step procedures for calibrating the VIC-1541. Only one calibration adjustment, to adjust the speed of the disk to 300 rpm, is provided in the VIC-1541. Perform the calibration procedure at the following intervals:

1. Every 6 months.

2. During the process of troubleshooting.

3. After a repair action.

5-2. Equipment Required

1. Small slotted screwdriver

2. Phillips screwdriver

3. Timing light (Refer to Appendix B)

NOTE

- Any strobe light with an accurate frequency of 50 Hz (+/- 1%) or 60 Hz (+/- 1%) may be used in place of the timing light.

4. Blank floppy disk (5 1/4 inch, single sided)

5-3. Preparation for calibration

1. Remove top cover. (Refer to Section6-DISASSEMBLY/REASSEMBLY)

2. Remove RFI shield. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

3. Disconnect P8 from J8.

4. Reinstall RFI shield. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

5. Remove bottom cover. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

6. Place disk drive on left-hand side. Use a thin book or magazine to prop up drive. (Refer to Figure 5-1).

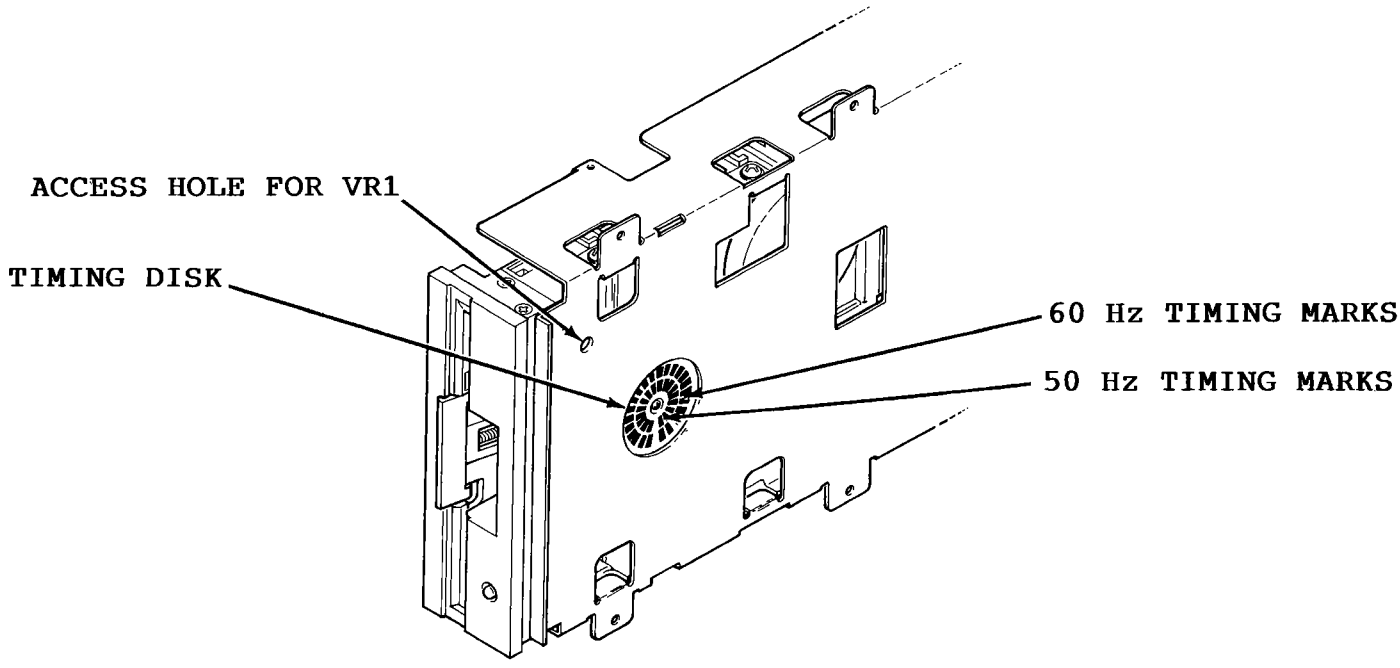


Figure 5-1. VIC-1541 Prepared for Calibration

5-4. Calibration

1. Connect VIC-20/COMMODORE 64 to video monitor or TV. (Refer to computer User's Guide for proper connection.)

2. Connect serial bus cable between P3 on VIC-1541 and serial bus connector on VIC-20/COMMODORE 64.

3. Connect AC power cord between J9 on VIC-1541 and AC outlet.

WARNING

- USE EXTREME CARE TO AVOID CONTACT WITH FRAME COMPONENTS. HIGH AC VOLTAGE POTENTIALS ARE PRESENT DURING CALIBRATION. THESE VOLTAGE POTENTIALS CAN CAUSE BODILY INJURY OR DEATH.

4. Place VIC-1541 power switch to ON.

5. Apply power to VIC-20/ COMMODORE 64.

6. If a VIC-20 is the computer being used, enter the following command:

```
OPEN 15,8,15,"UI-":CLOSE 15<Return>
```

7. Insert blank floppy disk into VIC-1541.

8. Plug timing strobe light into AC outlet. Position light near timing disk (Refer to Figure 5-1).

9. Enter following command into VIC-20/COMMODORE 64:

```
OPEN 15,8,15,"N0:CAL,01":CLOSE 15 <Return>
```

10. Adjust VR1 (Refer to Figure 5-1) until timing disk appears to stop.

NOTE

- If 60 Hz AC is being used, calibrate with the outer set of timing marks on the timing disk.
- If 50 Hz AC is being used, calibrate with the inner set of timing marks on the timing disk.
- If further time is required to adjust VR1, go back to Step 9 and re-enter command given.

11. After drive motor has stopped, place VIC-1541 power switch to OFF.

12. Remove serial bus cable and AC power cord.

13. Reassemble the VIC-1541. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

5-5. **Mechanical Alignment of Track #1 Stop**

5-5-1. General

This procedure adjusts the Track #1 Stop. The Track #1 Stop is used by the computer in the VIC-1541 for only two purposes:

1. Formatting a blank floppy disk ("New" command).

2. Soft error recovery.

The procedure that follows should only be used after carefully verifying that the rest of the VIC-1541 is properly operating, in accordance with the procedures given in Troubleshooting-Part 2.

5-5-2. Preparation for Mechanical Alignment.

1. Remove all external cables from VIC-1541.

2. Remove upper cover (Refer to Section 6-DISASSEMBLY/REASSEMBLY).

3. Remove RFI Shield (Refer to Section 6-DISASSEMBLY/REASSEMBLY).

4. Remove Disk Controller PC Board (Refer to Section 6-DISASSEMBLY/REASSEMBLY).

5. Remove Drive Unit (Refer to Section 6-DISASSEMBLY/REASSEMBLY).

6. Reconnect J1 to P1, J2 to P2, J5 to P5, J6 to P6 and J7 to P7 in such a manner that access is still allowed to the Track #1 Stop adjustment. (See Figure 5-2)

CAUTION

- DO NOT ALLOW PATHWORK ON DISK CONTROLLER PC BOARD TO CONTACT THE FRAME OR DRIVE UNIT ASSEMBLIES. USE AN INSULATING RUBBER MAT, IF NECESSARY, TO INSULATE THE DISK CONTROLLER PC BOARD FROM THESE ASSEMBLIES.

5-5-3. Mechanical Alignment

1. Connect serial bus cable between P3 and VIC-20/COMMODORE 64.

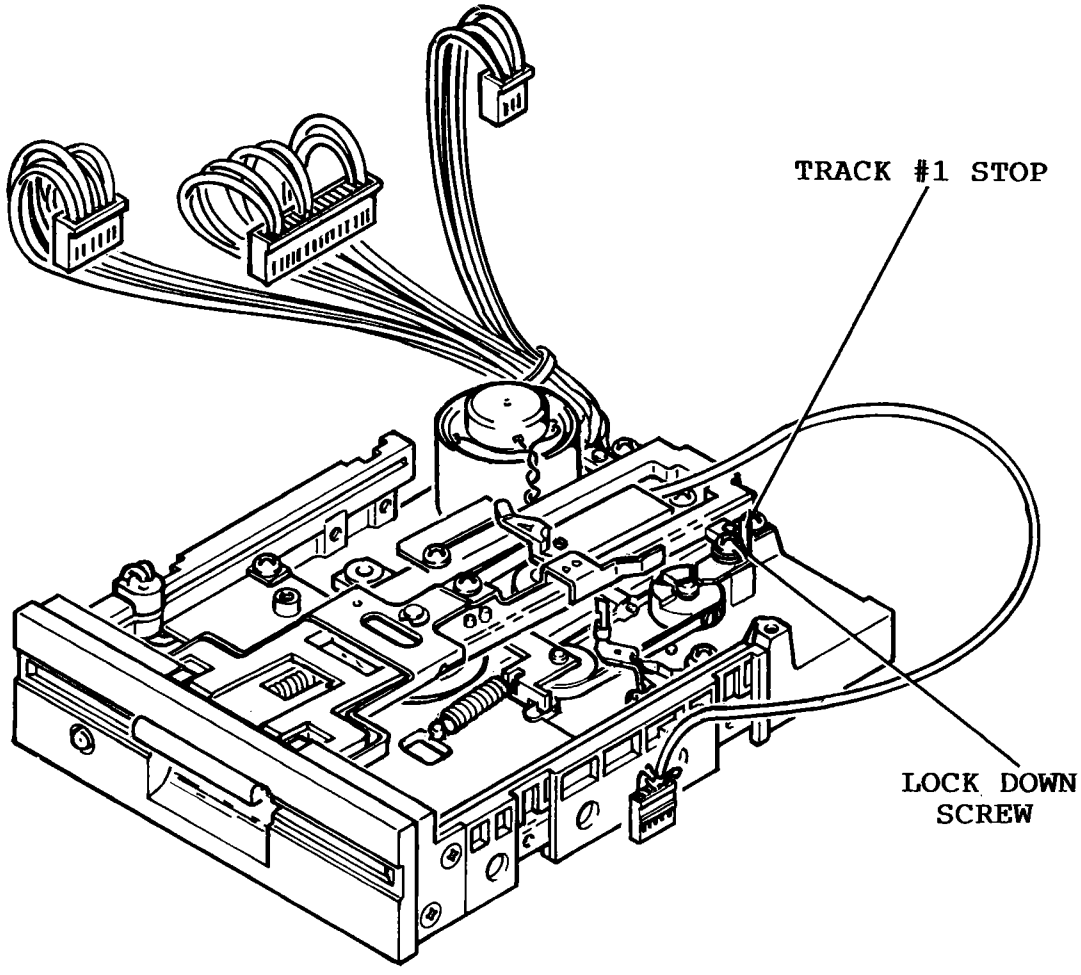


Figure 5-2. Track #1 Stop Adjustment.

2. Connect AC line cord between J9 and AC outlet.

WARNING

- DO NOT CONTACT THE FRAME ASSEMBLY OR WIRING. THE VOLTAGE POTENTIALS PRESENT ON THESE PARTS COULD CAUSE SEVERE INJURY OR DEATH.

3. Place VIC-1541 power switch to ON and place power switch on computer being used to ON.

NOTE

- If the VIC-20 is the computer in use, enter the following command: OPEN 15, 8, 15, "U-": CLOSE 15 <return>.

4. Load the Display T&S program into the computer. This program may be loaded from the Test Demo disk or it may be manually entered from the keyboard (The Display T&S program is listed in Appendix C of the VIC-1541 Single Drive Floppy Disk User's Manual.).

5. Place a factory recorded floppy disk into the VIC-1541.

6. Enter "RUN" <return> into the computer.

7. When the Display T&S program asks for a Track and Sector, enter Track 1, Sector 1.

8. After the head settles and the Display T&S program begins displaying Track information, adjust the Track #1 Stop adjustment in the following manner (See Figure 5-2):

a. Loosen the adjustment lock-down screw.

b. Carefully adjust the Stop until it just touches the potrusion on the stepping motor hub.

NOTE

- Do not disturb position of the stepping motor shaft.

c. Tighten the adjustment lock-down screw.

9. Place VIC-1541 and VIC-20/COMMODORE 64 power switches to OFF.

10. Reassemble the VIC-1541 (Refer to Section 6-DISASSEMBLY/REASSEMBLY).

SECTION 6
DISASSEMBLY/REASSEMBLY

Section 6-DISASSEMBLY/REASSEMBLY

WARNING

- REMOVE AC POWER CORD BEFORE ANY DISASSEMBLY IS ATTEMPTED.

NOTE

- The only tool required for disassembly or reassembly is a Phillips screwdriver.

6-1. **Disassembly** (Refer to Figure 6-1)

1. Remove top cover (Item 1) by removing four screws (Item 7) securing top cover to bottom cover (Item 8).

2. Remove RFI shield (Item 2) by:

   a. Removing two screws (Item 4) and two lockwashers (Item 3) securing RFI shield to Frame (Item 5).

   b. Lifting RFI shield and tilting it to the right to allow the two dimples on the right side of the RFI shield to clear their mating holes on the Frame.

CAUTION

- DO NOT PULL RFI SHIELD AWAY FROM THE FRAME BEFORE COMPLETING THE FOLLOWING STEP OR DAMAGE TO THE WIRING MAY RESULT.

   c. Rotating RFI shield to the left and disconnecting J8 from P8.

3. Remove Disk Controller PC Board (Item 11) by:

   a. Removing eight screws (Item 13) and eight lockwashers (Item 12) securing Disk Controller PC Board to Frame.

   b. Disconnecting J5 from P5, J6 from P6, J7 from P7, J2 from P2 and J1 from P1.

4. Remove bottom cover (Item 8) from Frame by removing six screws (Item 10) securing bottom cover to Frame.

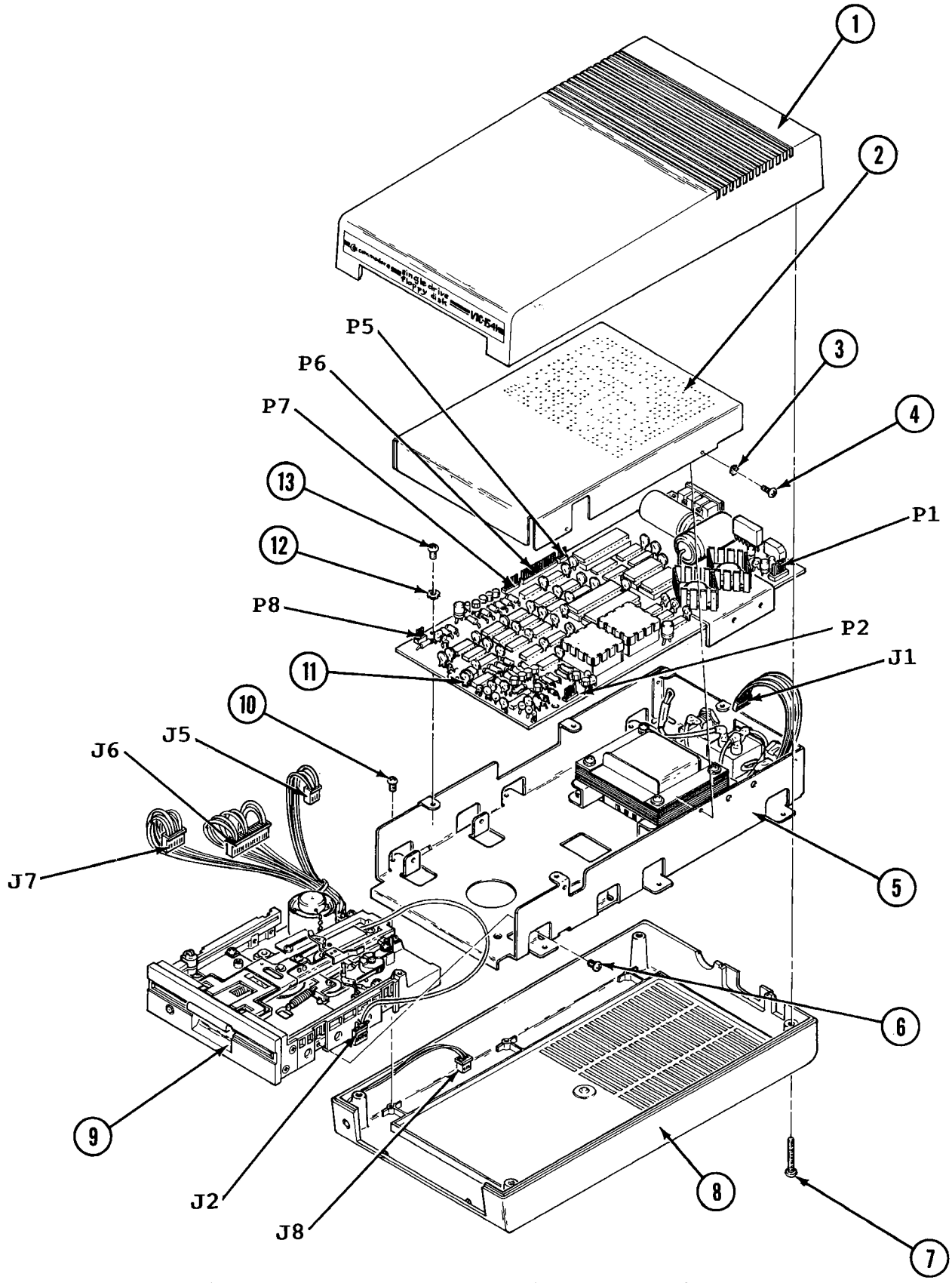


Figure 6-1. VIC-1541 Disassembly/Reassembly

5. Remove Drive Unit (Item 9) by:

   a. Removing four screws (Item 6) securing Drive Unit to Frame.

   b. Lifting Drive Unit up and out of Frame.

6-2. Reassembly

Reassembly of the VIC-1541 is accomplished in reverse order of the Disassembly procedures in Paragraph 6-1. Observe the following Caution during Reassembly.

CAUTION

- WHEN SECURING BOTTOM COVER TO FRAME AND DISK CONTROLLER PC BOARD TO FRAME, DO NOT OVER-TORQUE SCREWS OR DAMAGE TO PC BOARD OR BOTTOM COVER MAY OCCUR.

SECTION 7
PREVENTIVE MAINTENANCE

Section 7-PREVENTIVE MAINTENANCE

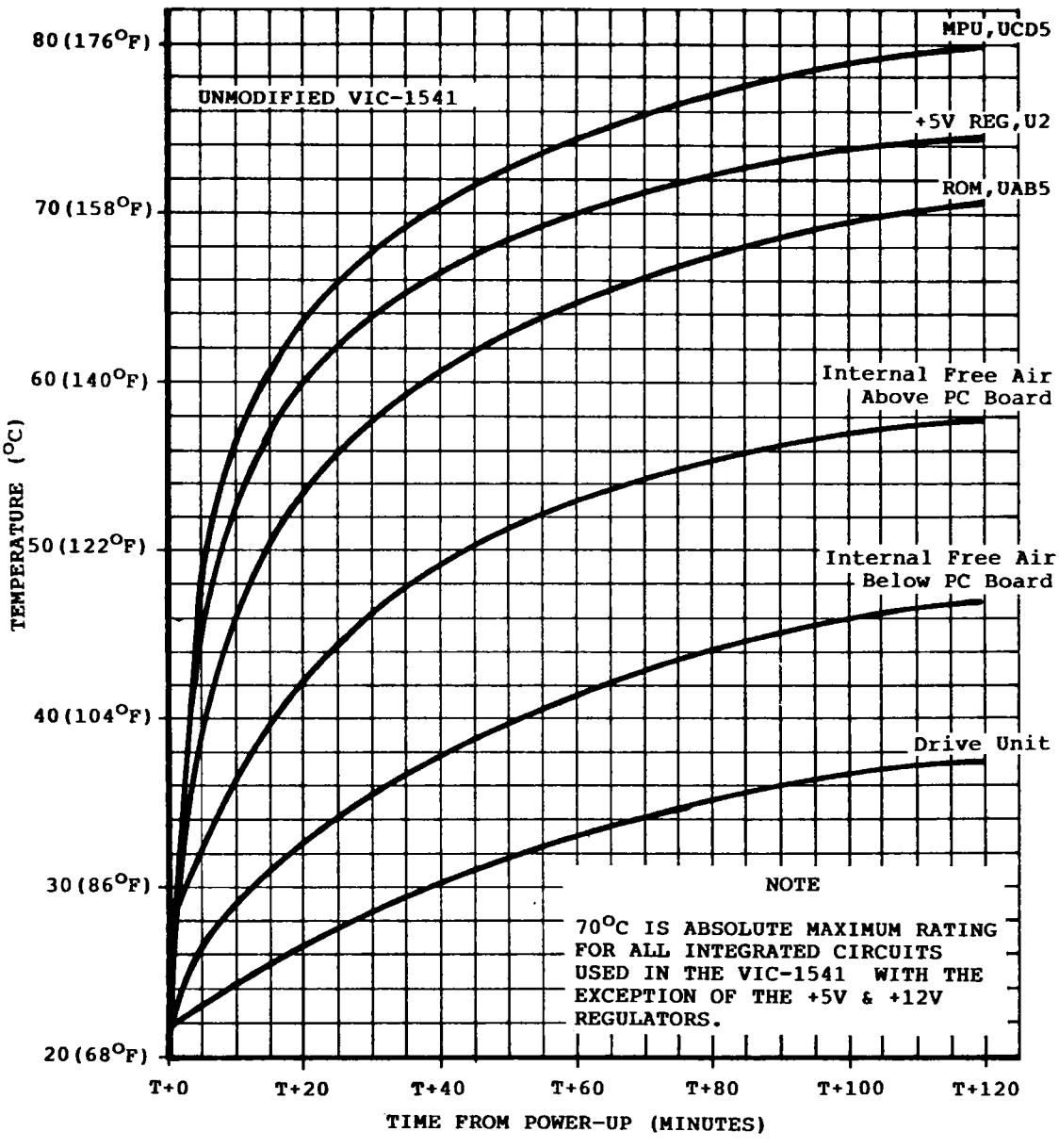
7-1. General

This section contains step-by-step procedures which will help to keep the VIC-1541 in peak operating condition. The procedures, which consist of cleaning and inspecting the internal sub-assemblies of the VIC-1541, should be performed every 6 months. Cleaning is necessary to remove dust and dirt which cause wear of moving parts, promote corrosion, and thermally insulate electronic parts. The last of these reasons for cleaning is the most important since the VIC-1541 already suffers from insufficient cooling. The graph in Figure 7-1 illustrates heat distribution within the VIC-1541. Notice that, after 40 minutes of operation, the 6502 microprocessor chip exceeds its absolute maximum temperature rating of +70°C. After 2 hours, the microprocessor's surface temperature escalates to +80°C. If dust and dirt are allowed to accumulate on the electronic components within the VIC-1541, the components will overheat even more because of the insulating effect of the dust.

One reason the VIC-1541 overheats is because the plastic case has a high insulating factor. The only escape for heat is the cooling vents located on top of the case. These vents are designed to prevent dust from entering the disk drive and should not be modified. To prolong the life of the VIC-1541, observe the following cautions:

CAUTION

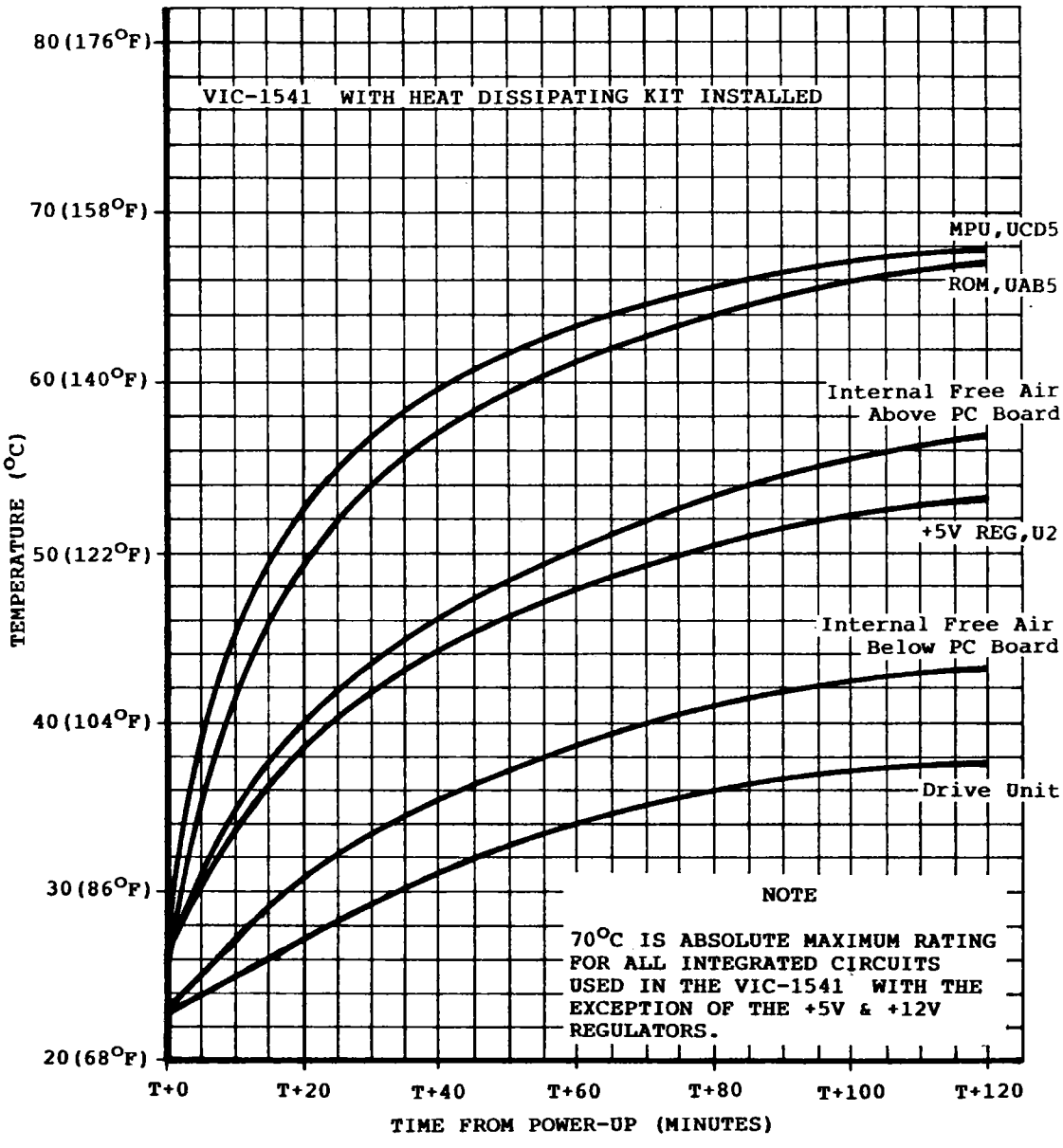
- DO NOT STACK VIC-1541'S ON TOP OF EACH OTHER.
- DO NOT PLACE BOOKS OR PAPERS ON TOP OF THE VIC-1541.
- DO NOT OBSTRUCT TOP OR BOTTOM COOLING VENTS ON THE VIC-1541.
- ALLOW AT LEAST 6 INCHES OF CLEARANCE BETWEEN VIC-1541 AND ADJACENT EQUIPMENT OR OTHER OBSTRUCTIONS TO AIRFLOW.
- DO NOT LEAVE FLOPPY DISK IN VIC-1541 FOR UNNECESSARILY LONG PERIODS OF TIME.
- TURN VIC-1541 OFF WHEN THE VIC 20/COMMODORE 64 IS NOT IN USE.



Test Conditions:

Unmodified VIC-1541* (S/N 138084) operating at idle (i.e., No serial bus connected, no motors turning). Temperature measured with Fluke Model 8024A DMM and 6 Type-K thermocouples attached to test surfaces with heat sink compound. Test ran in controlled 25°C (77°F) environment. Graph covers first two hours. After 11 hours readings were: MPU=80°C, +5V REG.=76°C, ROM=73°C, Internal Free Air Above PC Board=59°C, Internal Free Air Below PC Board=49°C, Drive Unit=39°C.

Figure 7-1. Unmodified VIC-1541.



Test Conditions:

VIC-1541* (S/N 138084) with **Heat Dissipating Kit** installed operating at idle (i.e., No serial bus connected, no motors turning). Temperature measured with Fluke Model 8024A DMM and 6 Type-K thermocouples attached to test surfaces with heat sink compound. Test ran in controlled 25°C (77°F) environment. Graph covers first 2 hours. After 11 hours readings were: MPU=69°C, +5V Reg.=55°C, ROM=69°C, Internal Free Air Above PC Boardd=58°C, Internal Free Air Below PC Board=46°C, Drive Unit=39°C.

Figure 7-2. VIC-1541 with **Heat Dissipation Kit** Installed.

CAUTION

- DO NOT USE A FAN TO COOL THE VIC-1541 OR ONE OF TWO THINGS WILL HAPPEN:

  A. INTAKE MODE-WHEN USING A FAN TO PUSH COOL AIR INTO VIC-1541, THE HOT EXHAUST AIR IS FORCED OVER THE FLOPPY DISK AND THE DRIVE UNIT, OVERHEATING THESE PARTS.

  B. EXHAUST MODE-WHEN USING A FAN TO PULL HOT AIR OUT OF VIC-1541, DIRT AND DUST ARE PULLED INTO THE DISK SLOT ON THE FRONT OF THE UNIT, CAUSING DUST MIGRATION.

- DO NOT OPERATE VIC-1541 IN AN ENVIRONMENT WHERE AMBIENT TEMPERATURES EXCEED 25°C (77°F).

The best method of cooling the VIC-1541 is to install a heat sink kit such as the **Heat Dissipation Kit** available from GOSUB OF SLIDELL and affiliated distributors. This kit is easy to install, does not promote dust migration, and keeps IC temperatures below their absolute maximum ratings. To see the difference an external heat sink can make, compare Figure 7-1 (Unmodified VIC-1541) with Figure 7-2 (VIC-1541 with **Heat Dissipation Kit** INstalled). The **Heat Dissipation Kit** will allow the VIC-1541 to operate safely even after 11 hours of operation. If your application of the VIC-1541 requires operating times in excess of 35 minutes, it is advisable to install a heat sink kit.

The **Heat Dissipation Kit** has been designed and tested by the author of this manual. He has authorized GOSUB OF SLIDELL as the distributor.

7-2. Equipment Required

1. Eraser

2. Lint-free cloth

3. Compressed air (15 psi. max.)/or a small clean brush

4. Head cleaning disk (optional)

7-3. Preparation for preventive maintenance

1. Disconnect AC power cable and serial bus cable(s) from VIC-1541.

2. Remove top cover of case. (Refer to Section6-DISASSEMBLY/REASSEMBLY)

3. Remove RFI shield. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

4. Remove disk controller PC Board. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

5. Remove bottom case half. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

7-4. Head Care

1. Clean and inspect read/write heads as follows:

NOTE

- Access may be gained to read/write heads by lifting pressure pad mount (Refer to Figure 7-3) from heads. Pressure pad mount can then be lifted to a vertical position with no resulting damage.

a. Remove any deposits from the heads with a lint-free cloth dampened (not wetted) with denatured alcohol.

CAUTION

- DO NOT USE EXCESSIVE FORCE ON HEADS.
- DO NOT SCRAPE DEPOSITS FROM HEADS. AVOID ABRASIVES OR ANY ACTIONS WHICH MAY DAMAGE THE HEADS.
- DO NOT USE A HEAD CLEANING DISK TO REMOVE LARGE DEPOSITS. SOME HEAD CLEANING DISKS MAY BECOME ABRASIVE AFTER EXCESSIVE USE.

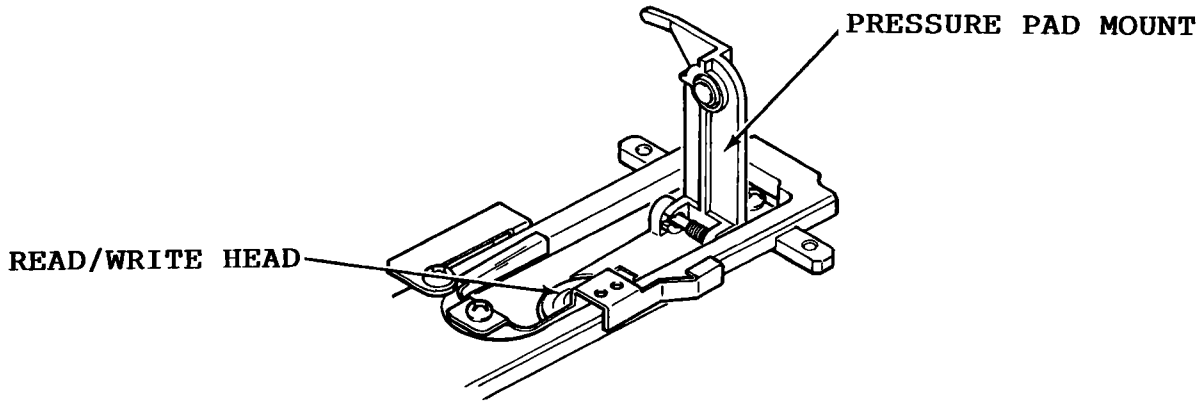


Figure 7-3. Access to read/write heads.

b. Inspect pressure pad on pressure pad mount for wear. Pad should be able to touch disk without allowing pressure pad mount to touch disk.

c. Inspect disk tension pads for excessive deformation or compression.

7-5. Cleaning and Inspection

1. Clean and inspect drive unit as follows:

   a. Carefully remove drive unit from frame. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

b. Remove dust from drive unit, using 15 psi of compressed air.

CAUTION

- NEVER EXCEED 15 PSI OF COMPRESSED AIR.
- DO NOT USE COMPRESSED AIR ON HEADS. SMALL PARTICLES MAY BE PRESENT IN AIRSTREAM WHICH COULD NICK OR CHIP HEADS.
- DO NOT REMOVE NOR LOOSEN SCREWS ON DISK DRIVE FOR SOLE PURPOSE OF CLEANING.
- AVOID PUTTING UNDUE STRAIN ON WIRE BUNDLES.
- ALWAYS USE EXTREME CAUTION WHEN HANDLING DRIVE UNIT.

NOTE

- If compressed air is not available, a small clean brush may be used to remove dust.

c. Any stubborn dirt may be removed with a damp lint-free cloth.

CAUTION

- USE DENATURED ALCOHOL TO DAMPEN CLOTH. NEVER USE WATER OR DETERGENTS ON DRIVE UNIT.

d. Inspect drive for signs of corrosion or physical damage.

e. Inspect drive belt for wear and fraying.

f. Clean components on drive servo circuit using 15 psi of compressed air.

CAUTION

- NEVER EXCEED 15 PSI OF COMPRESSED AIR.

NOTE

- If compressed air is not available, a small clean brush may be used to remove dirt.

g. Stubborn dirt on drive servo circuit may be removed with a damp cloth.

CAUTION

- USE DENATURED ALCOHOL TO DAMPEN CLOTH. NEVER USE WATER OR DETERGENTS ON DRIVE UNIT.
- DELIBERATE MOVEMENT (HOWEVER SLIGHT) OF DISCRETE COMPONENTS ON DRIVE SERVO CIRCUIT PC BOARD SHOULD BE AVOIDED.

h. Remove two screws which hold drive servo circuit board in place. Do not disconnect wires which attach to PC Board.

CAUTION

- DO NOT PUT UNDUE STRAIN ON WIRES WHICH CONNECT TO PC BOARD.
- AVOID EXCESSIVE MOVEMENT OF PC BOARD.

i. Using a clean lint-free cloth moistened with denatured alcohol, clean pathwork side of drive servo circuit PC Board.

CAUTION

- NEVER USE WATER OR DETERGENTS TO CLEAN PC BOARDS.

j. Inspect pathwork for corrosion. Remove corrosion by rubbing with an eraser, followed by cleaning with a lint-free cloth dampened with denatured alcohol.

k. Secure drive servo circuit PC Board back in place with two screws previously removed.

l. Inspect wire bundles for faulty insulation and for proper, secure connections.

CAUTION

- DO NOT CUT WIRE BUNDLE TIES FOR THE SOLE PURPOSE OF INSPECTION.
- DO NOT PUT UNDUE STRAIN ON WIRE BUNDLES.

m. Inspect connectors for corrosion and security of contacts.

2. Clean and inspect frame assembly as follows:

a. Remove dust using 15 psi of compressed air.

CAUTION

- NEVER EXCEED 15 PSI OF COMPRESSED AIR.

NOTE

- If compressed air is not available, a small clean brush may be used to remove dust.

b. Remove stubborn dirt with a damp lint-free cloth moistened with denatured alcohol.

CAUTION

- NEVER USE WATER OR DETERGENTS TO CLEAN FRAME ASSEMBLY.

c. Inspect F1 for proper size and rating. Fuse ratings are as follows:

115 VAC operation-1A

230 VAC operation-0.5A

d. Inspect insulation on unused tap of T1. The end of this wire should be insulated with electrical tape or heat shrink tubing as shown in Figure 7-4.

WARNING

- DO NOT CAP OFF WIRE AS SHOWN IN FIGURE 7-5. THIS METHOD MAY CREATE AN UNSAFE CONDITION WITH AGE.

e. Inspect remaining wires for frayed or faulty insulation.

f. Inspect wires for secure connections. All wires on frame assembly must be insulated with heat shrink tubing or equivalent.

g. Inspect frame for corrosion. Remove corrosion by gentle scraping, followed by cleaning with a lint-free cloth moistened with denatured alcohol.

h. Inspect connectors for cracked housings or loose pins.

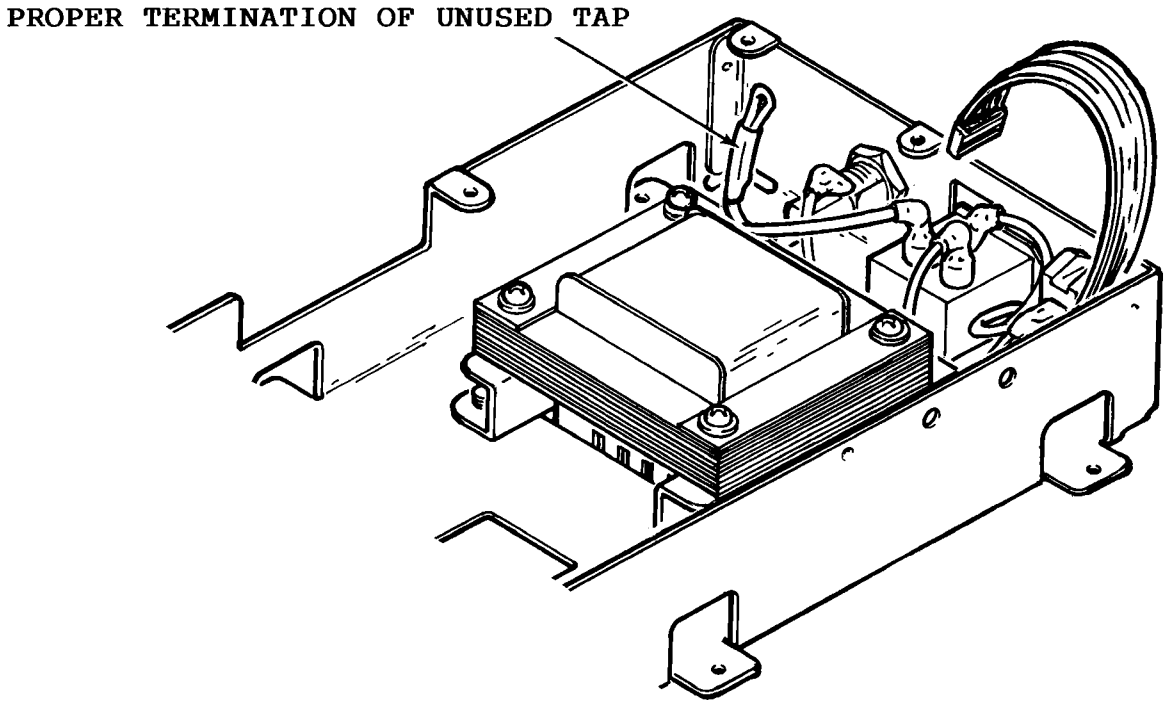


Figure 7-4. Proper Insulation of T1.

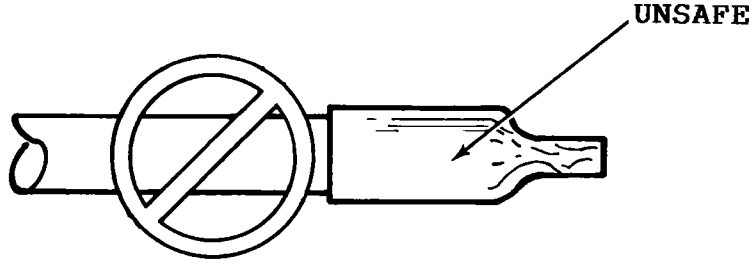


Figure 7-5. Improper Insulation of T1.

3. Clean and inspect disk controller PC Board as follows:

a. Remove dust and dirt using 15 psi of compressed air.

CAUTION

- NEVER EXCEED 15 PSI OF COMPRESSED AIR.

NOTE

- If compressed air is not available, a small clean brush may be used to remove dust.

b. Remove stubborn dirt with a lint-free cloth moistened with denatured alcohol.

CAUTION

- NEVER USE WATER OR DETERGENTS ON PC BOARDS.

c. Inspect PC Board assembly for corrosion. Remove any corrosion by gentle scraping, followed by cleaning with a lint-free cloth moistened with denatured alcohol.

d. Gently pry off two covers of shields on PC Board (Refer to Figure 9-6). Clean mating surfaces of covers and shields with an eraser.

e. Inspect components on PC Board as follows:

Capacitors-Check for leakage, swelling, deformation or any other obvious damage.

Resistors-Check for cracked, charred or broken bodies.

Semiconductors-Check for proper seating of socketed IC's. Check all IC's for obvious damage (cracks, loose pins, etc.).

CAUTION

- REFER TO MOS HANDLING PRECAUTIONS IN APPENDIX C BEFORE HANDLING SOCKETED IC'S.

f. Reinstall two covers on shields.

4. Reassemble VIC-1541. (Refer to Section 6-DISASSEMBLY/REASSEMBLY)

5. If desired, a head cleaning disk may be used at this time. Use the following procedure:

a. Connect AC power cord to J9.

NOTE

- Serial bus cables may be left disconnected.

b. Insert head cleaning disk.

CAUTION

- REFER TO MANUFACTURER'S INSTRUCTIONS FOR PROPER PREPARATION OF HEAD CLEANING DISK.

c. Place power switch to ON. Wait until red LED goes out.

d. Place power switch to OFF.

e. Again place power switch to ON and wait until red LED goes out.

f. Place power switch to OFF.

CAUTION

- DO NOT OPERATE DISK DRIVE EXCESSIVELY WITH HEAD CLEANING DISK IN PLACE AS EXCESSIVE HEAD WEAR MAY RESULT. SOME HEAD CLEANING DISKS BECOME ABRASIVE AFTER EXCESSIVE USE.

g. Remove head cleaning disk.

SECTION 8
TROUBLESHOOTING

Section 8-TROUBLESHOOTING

8-1. General

This section is divided into two major parts. Part 1 requires only a Multimeter (digital type is recommended) and will isolate a problem down to the sub-assembly level. Part 2 requires an oscilloscope in addition to the Multimeter and a frequency counter is also useful, if available. Part 1 is set up so that even an electronics novice can perform the procedures, while Part 2 will require more advanced skills. Whenever troubleshooting the VIC-1541, start with Part 1 and then proceed to Part 2 if the necessary equipment and skill level is available.

Part 1 consists of step-by-step procedures, with accompanying illustrations. Each step either asks a question or refers to the following step. When a question is asked, answer the question with a "Yes" or "No". Below each question are two blocks labeled "Yes" and "No". Follow the instructions in the appropriate block. The instructions will either lead to another step or will isolate the problem to a particular sub-assembly. At this point, the faulty sub-assembly may be replaced or the sub-assembly may be repaired down to the component level using the procedures in Part 2.

Part 2 consists of procedures for checking individual stages within the subassemblies. Perform the procedures in the sequence listed until an error or fault is discovered. Then isolate the faulty component and replace it.

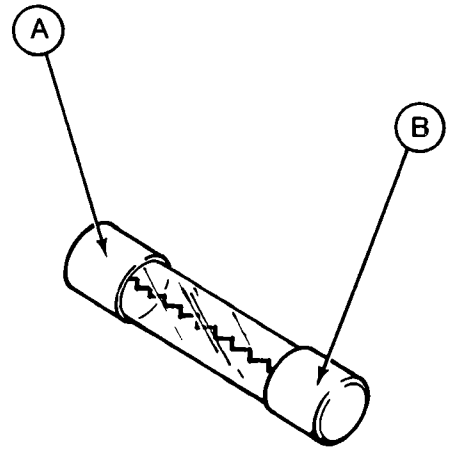
8-2. TROUBLESHOOTING-PART 1

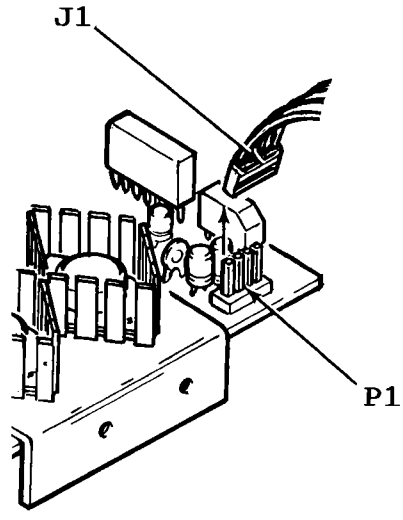
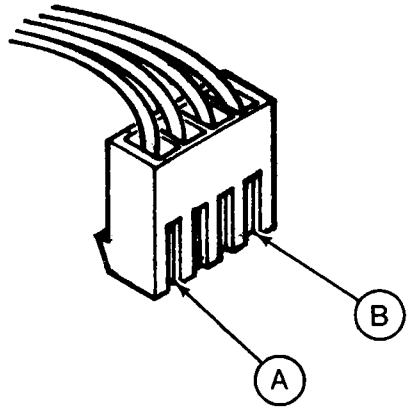
<table>
<tr><th>STEP</th><th colspan="2">PROCEDURE</th><th>ILLUSTRATION</th></tr>
<tr><td>1</td><td colspan="2">Remove AC line cord and serial bus cables. Remove top cover. Remove fuse from fuseholder. Measure resistance of the fuse as follows:

1. Set DMM (Digital Multimeter) to Ohms x 10 or Ohms x 100.

2. Connect common lead of DMM to one end of fuse (A).

3. Connect positive lead of DMM to other end of fuse (B).

Does DMM display less than 10 ohms?</td><td rowspan="2"> 
</td></tr>
<tr><td></td><td>YES</td><td>NO</td></tr>
<tr><td></td><td>Install fuse and proceed with Step 2.</td><td>Replace fuse with a new fuse of proper rating & size. Then proceed with Step 2.</td><td></td></tr>
</table>

STEP	PROCEDURE	ILLUSTRATION
2	Determine proper operation of the frame assembly as follows: 1. Disconnect J1 from P1. 2. Set DMM to measure Volts AC. 3. Connect negative lead of DMM to pin 1 of J1 (A). 4. Connect positive lead of DMM to pin 4 of J1 (B). 5. Connect AC line cord between J9 (the AC power receptacle) and an AC outlet. **WARNING** DO NOT CONTACT ANY AC DISTRIBUTION LINES. 6. Place power switch to ON. Does DMM display between 15 and 21.5 Vrms?	 

YES	NO
Proceed to Step 3.	Place power switch to OFF. Remove AC line cord. Fault lies in Frame Assembly. Repair or replace Frame Assembly.

<table>
<tr><th>STEP</th><th>PROCEDURE</th><th>ILLUSTRATION</th></tr>
<tr><td>3</td><td>Continue testing Frame Assembly as follows:

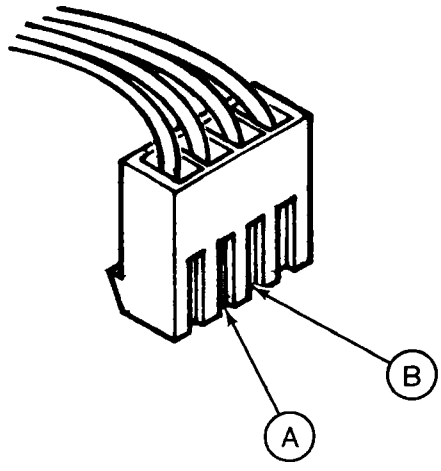
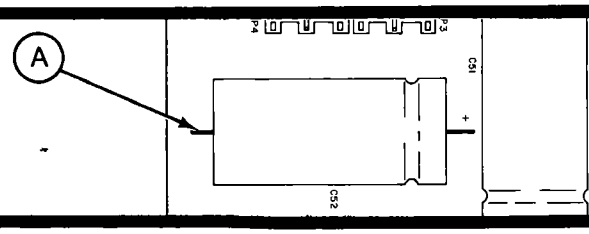
1. Place power switch to OFF.

2. Connect negative lead of DMM to pin 2 of J1 (A).

3. Connect positive lead of DMM to pin 3 of J1 (B).

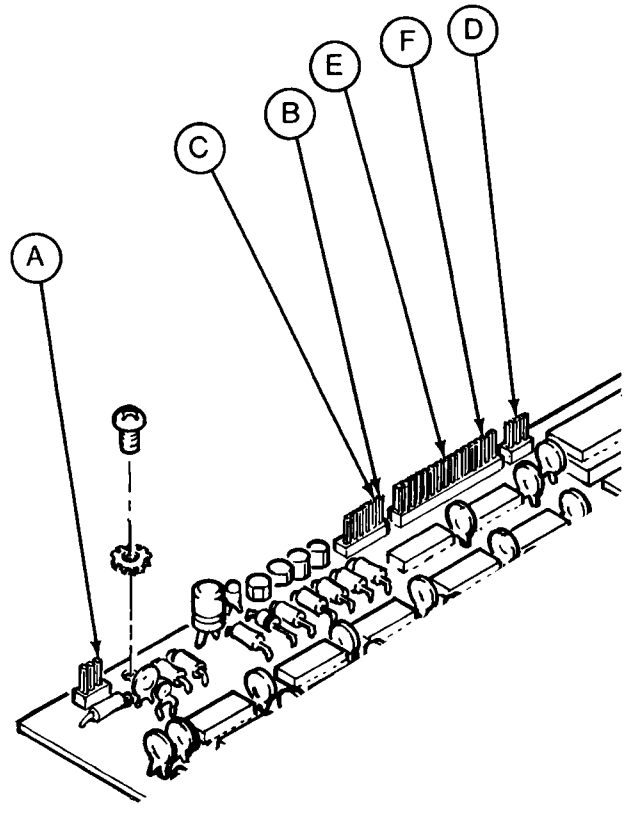
4. Place power switch to ON.

Does DMM display between 9.5 and 13.5 Vrms?

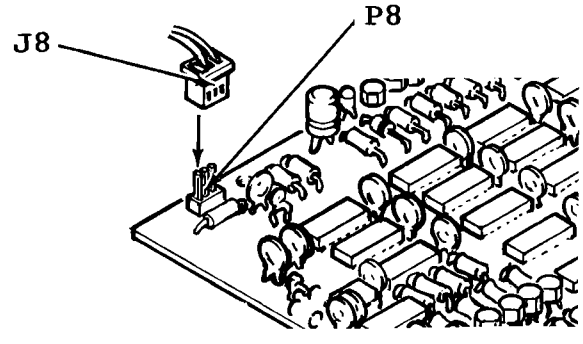
<table><tr><th>YES</th><th>NO</th></tr><tr><td>Frame Assembly appears to be working properly. Proceed to Step 4.</td><td>Place power switch to OFF. Remove AC line cord. Fault lies in Frame Assembly. Repair or replace Frame Assembly.</td></tr></table></td><td> 
</td></tr>
<tr><td>4</td><td>Place power switch to OFF. Remove AC line cord. Remove shield. Disconnect J2 from P2, J5 from P5, J6 from P6, J7 from P7 and J8 from P8. Proceed to Step 5.</td><td>SEE FIG. 9-2</td></tr>
<tr><td>5</td><td>Reconnect J1 to P1. Connect AC line cord to VIC-1541. Connect common lead of DMM to (-) side of C52 (A). Set DMM to 20 VDC range. Proceed to Step 6.</td><td> 
</td></tr>
</table>

<table>
<tr><th>STEP</th><th>PROCEDURE</th><th>ILLUSTRATION</th></tr>
<tr><td>6</td><td>Place power switch to ON. Measure tests points in table below. Touch positive lead of DMM to indicated test point. Verify that each measurement is within the minimum and maximum limits given.

<table>
<tr><th>Test Point</th><th>Min.</th><th>Max.</th></tr>
<tr><td>P8,pin1(A)</td><td>+4.6V</td><td>+5.25V</td></tr>
<tr><td>P7,pin1(B)</td><td>+11.4V</td><td>+12.6V</td></tr>
<tr><td>P7,pin2(C)</td><td>+11.4V</td><td>+12.6V</td></tr>
<tr><td>P5,pin2(D)</td><td>+11.4V</td><td>+12.6V</td></tr>
<tr><td>P6,pin8(E)</td><td>+4.75V</td><td>+5.25V</td></tr>
<tr><td>P6,pin2(F)</td><td>+4.6V</td><td>+5.25V</td></tr>
</table>
Are all measurements above within limits specified?

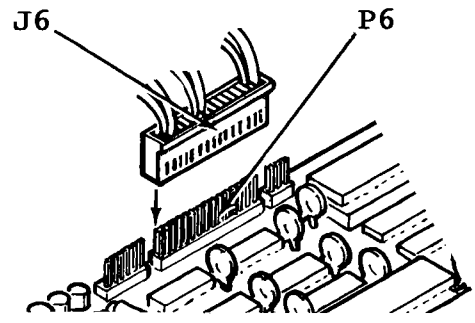
<table>
<tr><th>YES</th><th>NO</th></tr>
<tr><td>Place power switch to OFF. Proceed to Step 7.</td><td>Place power switch to OFF. Remove AC line cord. Fault lies in Disk Controller PC Board. Repair or replace.</td></tr>
</table></td><td> 
</td></tr>
<tr><td>7</td><td>Connect J8 to P8. Place power switch to ON.

Is green LED illuminated?

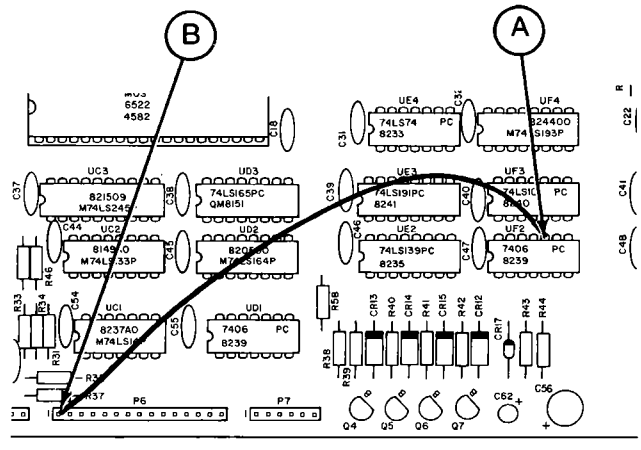
<table>
<tr><th>YES</th><th>NO</th></tr>
<tr><td>Place power switch to OFF. Proceed to Step 8.</td><td>Place power switch to OFF. Remove AC line cord. Fault lies in Case Assembly. Repair or replace.</td></tr>
</table></td><td> 
</td></tr>
</table>

<table>
<tr><th>STEP</th><th>PROCEDURE</th><th>ILLUSTRATION</th></tr>
<tr><td>8</td><td>Connect J6 to P6. Place power switch to ON.

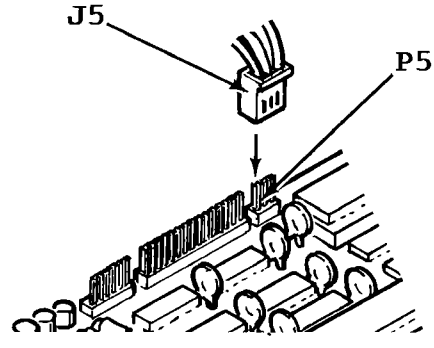
Does red LED come on momentarily?

<table><tr><th>YES</th><th>NO</th></tr><tr><td>Place power switch to OFF. Proceed to Step 10.</td><td>Proceed to Step 9.</td></tr></table></td><td> 
</td></tr>
<tr><td>9</td><td>Using a short piece of wire, carefully short pin 10 of UF2E (A) to pin 1 of P6 (B) while observing the red LED (Error/Access LED).

Does red LED illuminate?

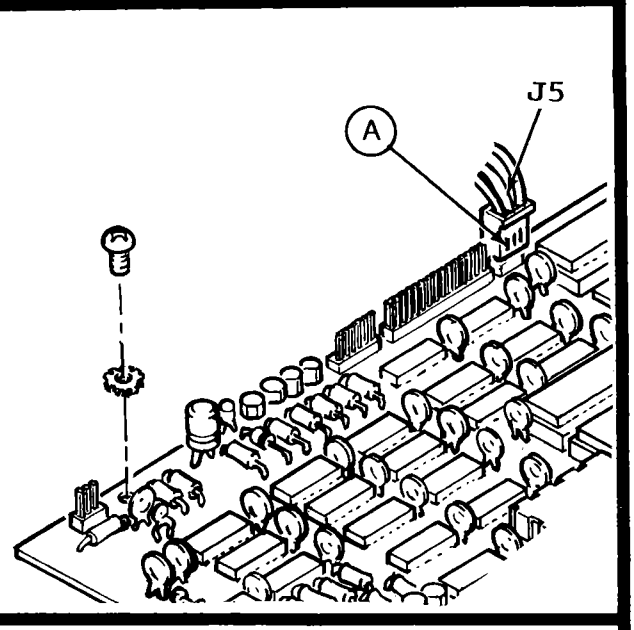
<table><tr><th>YES</th><th>NO</th></tr><tr><td>Place power switch to OFF. Fault lies in Disk Controller PC Board. Repair or replace.</td><td>Place power switch to OFF. Fault lies in Drive Unit. Repair or replace.</td></tr></table></td><td> 
</td></tr>
<tr><td>10</td><td>Connect J5 to P5. Place power switch to ON.

Does drive motor turn while red LED is on?

<table><tr><th>YES</th><th>NO</th></tr><tr><td>Place power switch to OFF. Proceed to Step 12.</td><td>Place power switch to OFF. Proceed to Step 11.</td></tr></table></td><td> 
</td></tr>
</table>

<table>
<tr><th>STEP</th><th>PROCEDURE</th><th>ILLUSTRATION</th></tr>
<tr><td>11</td><td>Connect positive lead of DMM to pin 3 of J5 (A). Observe DMM while placing power switch to ON.

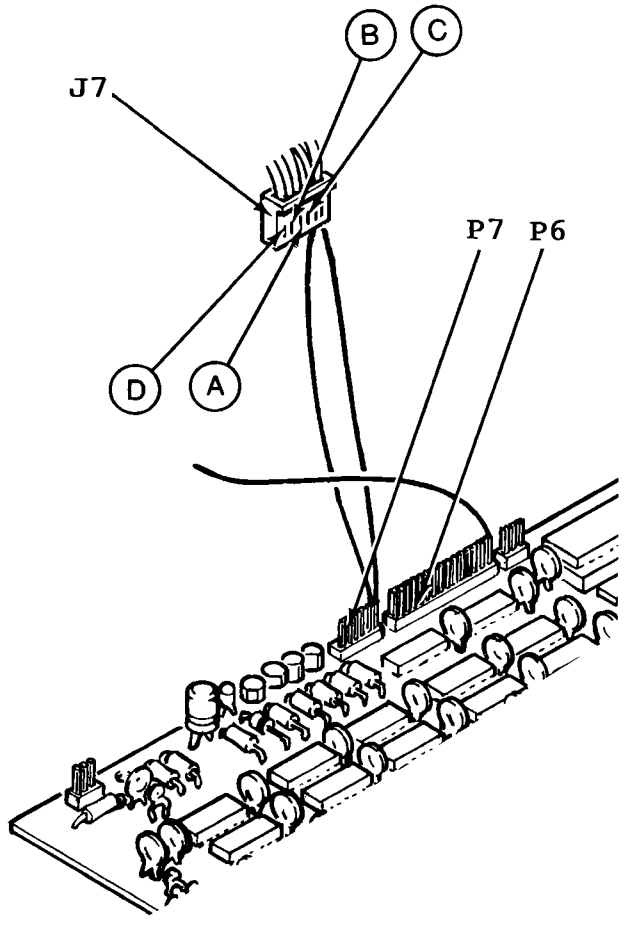
Does DMM indicate 0.0 to +0.8 V when the red LED is illuminated?

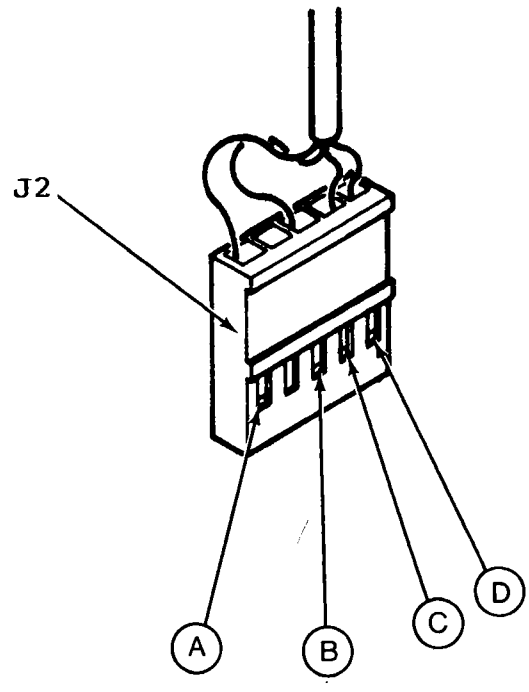
<table><tr><th>YES</th><th>NO</th></tr><tr><td>Place power switch to OFF. Fault lies in Drive Unit PC Board. Repair or replace.</td><td>Place power switch to OFF. Fault lies in Disk Controller PC Board Repair or replace.</td></tr></table></td><td> 
</td></tr>
<tr><td>12</td><td>Using two short lengths of wire, carefully connect pins 1 and 2 of J7 to pin 1 of P7. Place power switch to ON. Using a third piece of wire, short sequentially between pin 1 of P6 and each of the test points indicated below. Observe read/write head while shorting each test point.

1. J7, pin 4 (A)
2. J7, pin 5 (B)
3. J7, pin 3 (C)
4. J7, pin 6 (D)

Verify that the read/write head moves toward the front of the VIC-1541. Repeat the procedure in reverse order and verify that the read/write head moves toward the rear.

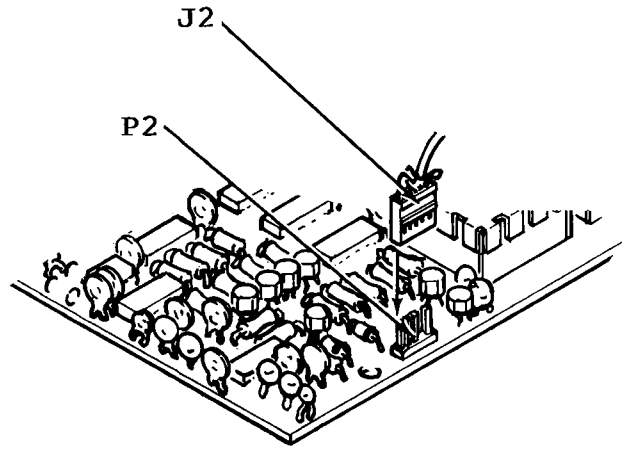
Does the read/write head move in the proper direction?

<table><tr><th>YES</th><th>NO</th></tr><tr><td>Place power switch to OFF. Proceed to Step 13.</td><td>Place power switch to OFF. Fault lies in Drive Unit.</td></tr></table></td><td> 
</td></tr>
</table>

STEP	PROCEDURE	ILLUSTRATION
13	Remove wires from J7. Connect J7 to P7. Remove negative lead of DMM from (-) side of C52. Set DMM to Ohms x 10 or Ohms x 100 range. Connect negative and positive leads of DMM to pins of J2 as indicated in table below. Verify resistances indicated on DMM are within limits given in table. (-) lead / (+) lead / Ohms Min. / Ohms Max. pin1(A) / pin5(D) / 29 / 39 pin1 / pin4(C) / 12 / 22 pin1 / pin3(B) / 23 / 33 **NOTE** This resistance check of the read/write head does not check its dynamic characteristics. If in doubt about the condition of the read/write head, refer to Part 2 of Troubleshooting. Are all resistances correct?	

YES	NO
Place power switch to OFF. Proceed to Step 14.	Fault lies in Drive Unit. Replace.

<table>
<tr><th>STEP</th><th>PROCEDURE</th><th>ILLUSTRATION</th></tr>
<tr><td>14</td><td>
Connect J2 to P2. Perform Calibration procedure in Section 5.

Is drive motor rotating at correct speed?
<table>
<tr><th>YES</th><th>NO</th></tr>
<tr><td>At this point the problem lies in the Disk Controller PC Board or in the Drive Unit. To determine which of the two sub-assemblies is bad, refer to Part 2 of Troubleshooting. Part 2 requires an oscilloscope and some technical experience. If you do not wish to attempt Part 2, try swapping the Disk Controller PC Board or the Drive Unit with a known good assembly and see if the problem is solved. Also, check assemblies for obvious signs of wear or damage.</td><td>Fault lies in Drive Unit. Replace.</td></tr>
</table>
</td><td> 
</td></tr>
</table>

8-3. TROUBLESHOOTING-PART 2

8-3-1. Frame Assembly

If it was determined in Troubleshooting-Part 1 that the frame assembly is faulty, the following guidelines are provided to assist in troubleshooting the frame assembly.

WARNING

- REMOVE THE AC LINE CORD PRIOR TO REPAIRING THE FRAME ASSEMBLY.

Using an ohmmeter, verify proper operation of the power switch (S1), the fuse and the fuseholder (F1), and the AC line connector (J9). Verify terminals 1 and 3 of J9 are not shorted to each other or to the chassis. Inspect and test continuity of the wiring and the AC line cord with an ohmmeter. If none of the above checks reveal a fault, the problem lies in the transformer (T1).

8-3-2. Power supply

After checking the frame, the power supply should be checked next. Test the power supply using a Voltmeter and the table below.

NOTE

- The chassis ground is isolated from the circuit ground in order to prevent ground loops. When making any voltage measurement relative to ground, connect the common lead of the Voltmeter to the (-) side of C52 or to one of the shields around the Timing Circuits.

If an oscilloscope is available, it may be used to check the ripple on the supply lines. Use AC coupling and trigger on the AC line.

STEP	TEST POINT	VOLTAGE	RIPPLE
1	(+) side of C51	+21V(+/-3V)	<0.3V
2	(+) side of C52	+10V(+/-2V)	<0.8V
3	anode of CR4	+5V(+/-0.25V)	<50mV
4	anode of CR2	+12V(+/-0.6V)	<70mV

8-3-3. **Timing Circuits**

After checking the power supply, next check the Timing Circuits. Use Figure 8-1 to check the operation of the 16 MHz oscillator. Use Figures 8-2 and 8-3 to check the operation of the divide by 16 frequency divider. Figure 8-3 is the 1 MHz microprocessor clock. Use Figure 8-4 to check the operation of the programmable divider as outlined in this paragraph. Use the "Display Track and Sector" program printed in the VIC-1541 User's Manual. Load and run the program (if possible) and when the program asks for track and sector, enter the desired track per Figure 8-4 and sector 1. If the program cannot be loaded or executed, change the states of pins 1 and 15 of UE7 as follows:

1. Place COMMODORE 64/VIC-20 power switch to OFF.

2. Place VIC-1541 power switch to OFF and allow 30 seconds for capacitors to discharge.

3. Remove UCD4 from its socket.

CAUTION

- OBSERVE MOS HANDLING PRECAUTIONS. SEE APPENDIX C.

4. Place VIC-1541 power switch to ON.

5. Change the states of pins 1 and 15 of UE7 by jumpering pins 1 and 15 to ground or to +5V. Check all four conditions listed in Figure 8-4.

6. Place VIC-1541 power switch to OFF and allow 30 seconds for capacitors to discharge.

7. Remove jumpers and install UCD4.

CAUTION

- OBSERVE MOS HANDLING PRECAUTIONS. SEE APPENDIX C.

8-3-4. **Computer**

After checking the Timing Circuits, it is next necessary to check the operation of the computer, which is required to be in operating order to check the remaining circuits. However, since the computer is the most difficult circuit to troubleshoot, first try initializing the computer and communicating with it over the serial bus. If this is possible, the computer probably works, and you can proceed to the Read Circuit. If this is not possible, proceed with the following instructions.

With power OFF, check out UAB1 and UCD4 by swapping them between their 40-pin sockets. Then, with power ON, see if the problem has changed characteristics. If so, one of the 6522's is faulty.

Next, measure the voltage on the reset line (UD1D, pin 8). Verify that voltage is greater than 4.0 volts. Now the serial bus interface, the address decoder and the read/write circuits may be checked. First, remove the serial bus cable(s) and the following socketed IC's: UAB1, UCD4, UCD5, UAB4, and UAB5. Then, using a voltmeter, short lengths of wire and the Disk Controller Schematic, statically test the following IC's: UB7, UB6A, UB6B, UB8, UG2B, UC1F, UD1C, UC1B, UD1B, UC1A, and UD1A. Use the wire to insert a logic low at one of the pins of the empty IC sockets by connecting the pin to ground. To insert a logic high, leave the pin of the IC socket open. Use the voltmeter to measure the output of the logic gate being tested.

The RAM chips, UA2, UA3, UB2 and UB3, are difficult to test. The easiest method would be to obtain a known good RAM and sequentially swap the known good RAM with each of the four RAMs and observing th results. If the problem clears up, the replaced RAM is bad. If the problem does not clear up, the RAM chips are probalbly not at fault. Installation of IC Sockets in RAM locations makes this method simpler. Installing sockets may reduce the reliability of the VIC-1541 by a small degree, so it may be desired to remove the sockets and reinstall the IC's after locating any problems.

If a problem in the computer hasn't shown up by this point and a problem indeed exists in the computer, then the problem is in UAB4, UAB5 or UCD5. To isolate a problem in these chips without the use of a logic analyzer, swap the IC's with known good IC's.

8-3-5. **Read Circuit**

To test the video amplifiers, connect one side of the differential signal to channel A of oscilloscope and the other side of the differential signal to channel B. Invert channel B and set the display mode to A+B. The necessary waveforms may be obtained using the Display Track and Sector program from the VIC-1541 User's Guide. Enter the program into the VIC-20/COMMODORE 64 and execute it. When prompted, select Track 1, Sector 1.

NOTE

- If VIC-1541 under test is assigned a device number other than 8 (Refer to Section 3-Initial Configuration), the Display Track and Sector program must be modified by changing all device number references in the OPEN statements from 8 to the correct device number.

Short pin 3 of P5 to ground. This will cause the motor to turn.

NOTE

- The read amplifiers may oscillate when not in use, but this is a normal occurrence.

Using the oscilloscope set-up described above and Figure 8-22, verify the input from the head is per Figure 8-21. The DC bias at pins 1 and 14 of UH7 is approximately 6 volts. Refer to Figure 8-23 for proper oscilloscope display at pins 7 and 8 of UH7. With oscilloscope connected to output of the first video amplifier, check mechanical alignment as follows:

NOTE

- Use a factory recorded disk or a disk which was formatted on a VIC-1541 that is known to be properly aligned.

Set oscilloscope to 100 mS/Div. Observe overall envelope of video and compare it with following general guidelines:

Flat, with constant amplitude-correct mechanical alignment.

Random changes in overall amplitude-incorrect tension or pressure on head.

Sinewave, 2 div/cycle-drive hub off center.

Sinewave with harmonics-gross misalignment of hub.

Low in amplitude-dirty head, incorrect track position, incorrect head pressure, incorrect tension, misalignment of disk seating plane or axial misalignment of the read/write head. Also check first video amplifier and the heads for proper electrical operation.

NOTE

- No provision is made on the VIC-1541 Drive Unit for head alignment. If a problem is clearly revealed as a head alignment problem, the Drive Unit must be replaced.

Return oscilloscope sweep to previous setting.

Verify bias voltage at the junction of R16 and R17 is approximately 6 volts. Verify the output of pins 7 and 8 of UH5 are per Figure 8-24. Verify bias voltage on pins 2 and 3 of UH4 is approximately 6 volts. Verify waveform at pin 7 of UH4 is at least 4 volts peak to peak. Check wide and narrow pulse widths out of UG2D per Figures 8-25 and 8-26, respectively. Check operation of single shot, UG3A, per Figures 8-27 and 8-28. Check operation of UF6A and UG2A per Figures 8-29 and 8-30. Check final output of read circuits at pin 10 of UG3B. Verify pulse width is per Figures 8-31 and 8-32. Remove jumper wire from P5.

8-3-6. **Encoder/Decoder**

NOTE

- The Encoder/Decoder waveforms referred to in this paragraph have been simplified for clarity of presentation. The actual waveforms displayed will contain some jitter. Some waveforms are labeled "random pulses" in lieu of a frequency. For these waveforms only the first pulse displayed will be clear and the rest of the pulses will not be synchronized with the oscilloscope sweep.

- All of the timing values used are applicable using the track 0 thru 17 clock (i.e., 1.250 MHz). To assure proper clock state, verify pins 1 and 15 of UE7 are logic 1's. If either pin is a logic low, set them high by accessing Track 1, Sector 1 by using the Display Track and Sector program in the VIC-1541 User's Guide.

After testing the Read Circuits, test the Encoder/Decoder Circuit in the following manner. Verify read/write line (UF5A, pin 2) is greater than 4 volts. Verify proper operation of UF4 using test points and results listed in Figures 8-5 thru 8-10. Test UE3 per Figures 8-11, 8-12, and 8-13. Verify proper operation of UF3 in accordance with Figures 8-14, 8-15, and 8-16. Verify proper operation of UE5A per Figure 8-17. Only the first pulse displayed on the oscilloscope will be discernible, in most instances. Check the outputs of UD2 and UE4 using Figure 8-18. Check the operation of UD3 per Figure 8-19. Check the operation of UF5B per Figures 8-20 and 8-21. To check the operation of UC2, insert a floppy disk into the VIC-1541, attempt to load the directory of the disk into the VIC-20/COMMODORE 64 and observe pin 9 of UC2 while the directory is being transferred. Verify that active low outputs

are present on pin 9 of UC2 during the transfer.

8-3-7. **Write Circuit**

After testing the Encoder/Decoder Circuit, test the Write Circuit in the following manner. Connect oscilloscope channel B to the read/write line (UF5A, pin2). Trigger on channel B, using (-) trigger. Insert a blank floppy disk into the VIC-1541 and enter the following command: OPEN 15,8,15,"N0:A,11":CLOSE 15.

NOTE

- All Write Circuit logic levels given hereafter apply only during the time the read/write line (channel B) is low.

Using a Voltmeter, verify write protect line from the Optics Circuit is at a logic 0 (meaning no disk installed or write protect notch is uncovered). Using channel A of the oscilloscope, check UF5D for proper operation. Pin 11 of UF5D will be low when the read/write line is low. Using channel A of the oscilloscope, verify the cathode of CR9 displays a logic 0 when the read/write line is low. Using channel A of the oscilloscope, verify pin 8 of UF5C goes high when the read/write line is low. Verify pin 8 of UG2C, the collector of Q9, and the collector of Q10 all exhibit the same timing characteristics as pin 8 of UF5C. Connect channel A of oscilloscope to pin 9 of UF6B. Verify the output of pin 9 is a square wave. Connect channel A of oscilloscope to the cathode of CR11. Connect channel B to cathode of CR6. Verify oscilloscope displays bursts of data similar to Figure 8-33. Notice that channel A and channel B are 180^{o} out of phase. Test the Write Protect circuit by bringing floppy disk halfway out of the VIC-1541. Using a Voltmeter, verify that pin 8 of UC1D is at a logic low. Verify that the output of UF5D is a logic high.

8-3-8. **Track Select Circuit**

The Track Select Circuit may be tested in the following manner. Insert a blank floppy disk into the VIC-1541. Enter the following command into the VIC-20/COMMODORE 64: OPEN 15,8,15,"N0:A,11". **DO NOT PRESS RETURN UNTIL INSTRUCTED TO DO SO.** Connect channel B of oscilloscope to pin 13 of UF2F. Connect channel A of oscilloscope to collector of Q5. Press RETURN on VIC-20/COMMODORE 64 while observing oscilloscope. Verify both channels exhibit identical timing characteristics. Verify signal on channel A is at least 11 volts peak to peak. Repeat the procedure above to test the remaining three drivers (UF2C and Q6, UF5B and Q4, UF2A and Q7). Connect channel B of oscilloscope to pin 9 of UF2D. Connect channel A to pin 8 of UF2D. Start the drive motor by attempting to load the directory. When channel B goes high, channel A should go low. Connect channel A of oscilloscope to pin 3 of P5. Start drive motor by attempting to read the directory. Verify that channel A goes low when channel B goes high.

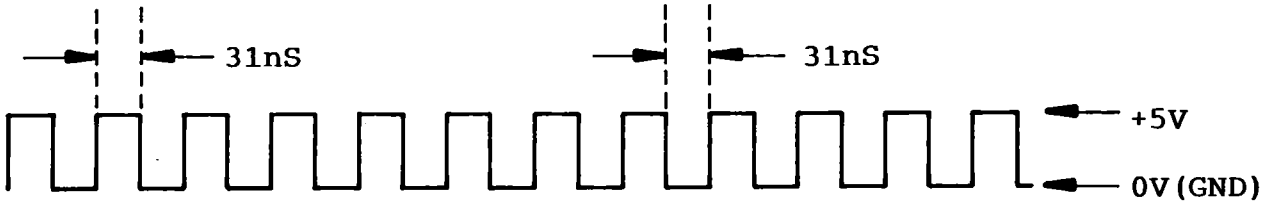
8-3-9. **Optics Circuit**

Test the Optics Circuit in the folowing manner. Measure the voltage at pin 12 of P6. With no floppy disk in the VIC-1541, voltage should be less than one volt. Insert a floppy disk that has the write protect notch covered. Voltage at pin 12 of P6 should increase to greater than 4 volts. Determine the current drawn by the LED's by measuring the voltage across R45, R35 and R36 and then applying Ohm's Law. Turn on the access/error LED by entering the following command into the VIC-20/COMMODORE64: OPEN 15,8,15,"N0:A,11". Verify that the access/error LED is illuminated.

8-3-10. **Drive Motor/Servo Circuit**

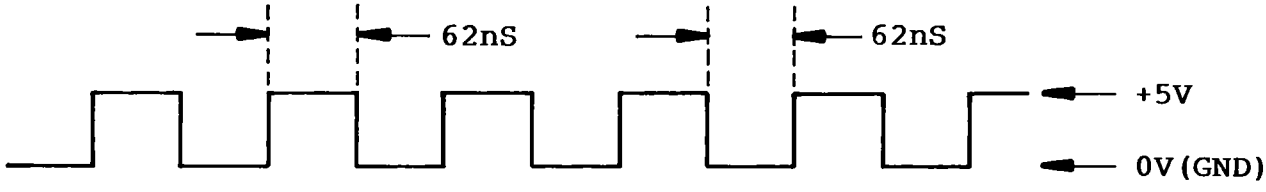
Test the Drive Motor/Servo Circuit in the following manner. Using a voltmeter, measure voltage at E1 (brown wire). Verify voltage is +12 volts (+/- 0.6 volts). Measure voltage at E2 (orange wire). Verify voltage is greater than 4 volts (motor off condition). Measure voltage at collector of Q1 (on Drive Motor/Servo Circuit PC Board). Verify voltage is less than 0.5 volts. Start motor by entering the following command into the VIC-20/COMMODORE 64: OPEN 15,8,15,"N0:A,11". Verify proper operation of tachometer and of rectifiers CR1, CR2, CR3 and CR4. Verify display is per Figure 8-34. Using Voltmeter, verify voltage at E6 is approximately 6 volts.

8-4. TROUBLESHOOTING-WAVEFORMS



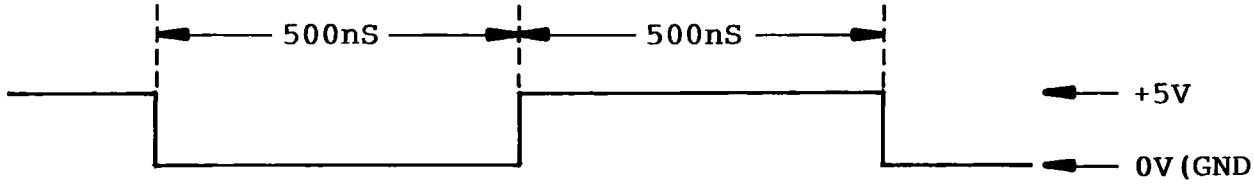
UC6,pin 8 FREQUENCY=16.000 MHz

Figure 8-1.



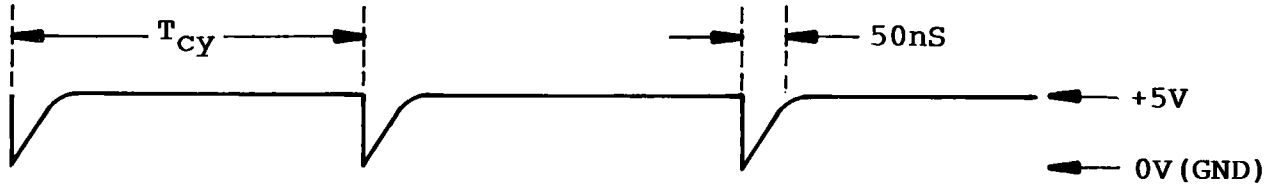
UC6,pin 5 FREQUENCY=8.000 MHz

Figure 8-2.



UC6,pin 12 FREQUENCY=1.000 MHz

Figure 8-3.



Track Selected	UE7,pin 1	UE7,pin 15	T_{cy}	Frequency MHz
1-17	+5V	+5V	812nS	1.2307
18-24	+5V	0V	875nS	1.1428
25-30	0V	+5V	937nS	1.0666
31-35	0V	0V	1.0uS	1.0000

UE7,pin 12

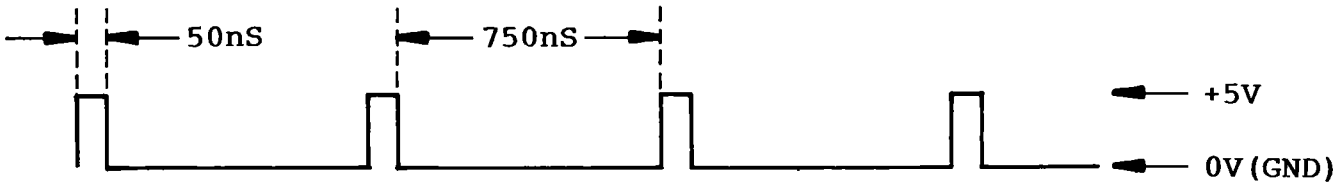
Figure 8-4.

NOTE

- Use + trigger when synchronizing oscilloscope.

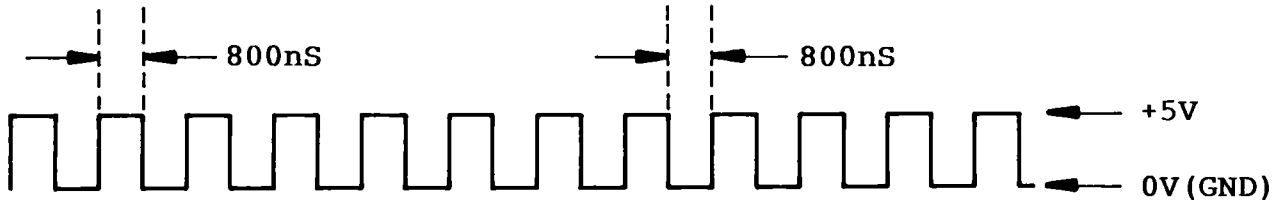
UF4,pin 14 Random Pulses

Figure 8-5.



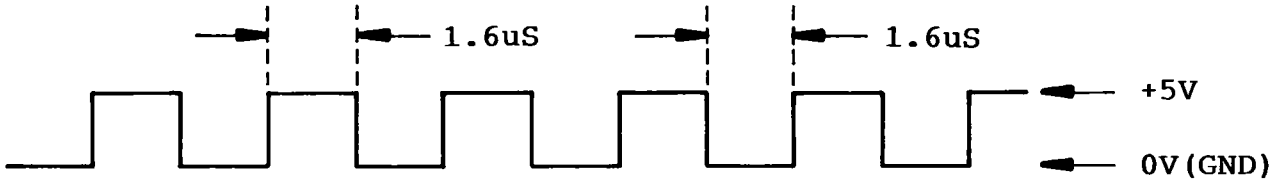
UF4,pin 5 FREQUENCY=1.25 MHz

Figure 8-6.



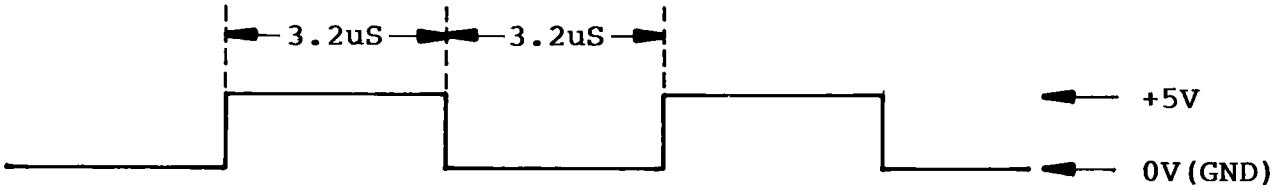
UF4,pin 3 FREQUENCY=625.000 kHz

Figure 8-7.



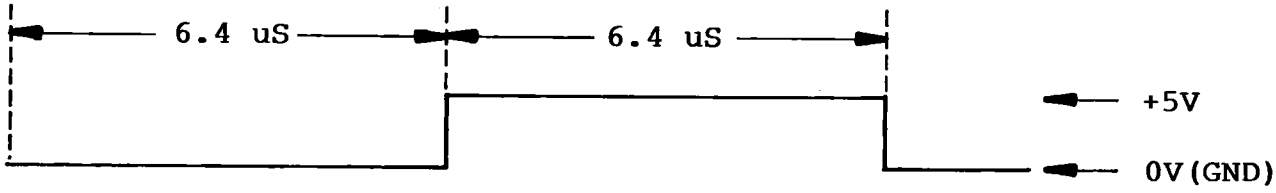
UF4,pin 2 FREQUENCY=312.50 kHz

Figure 8-8.



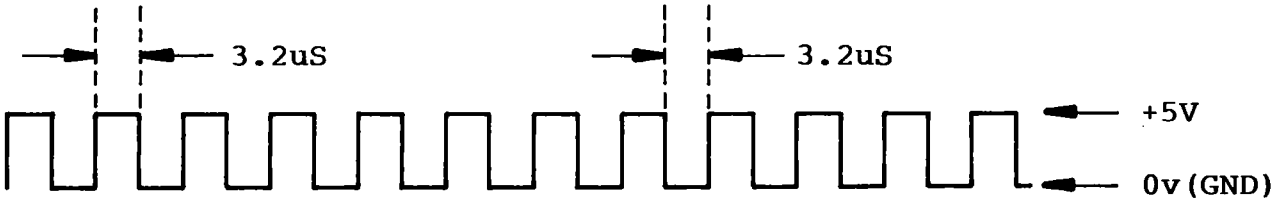
UF4,pin 6 FREQUENCY=156.25 kHz

Figure 8-9.



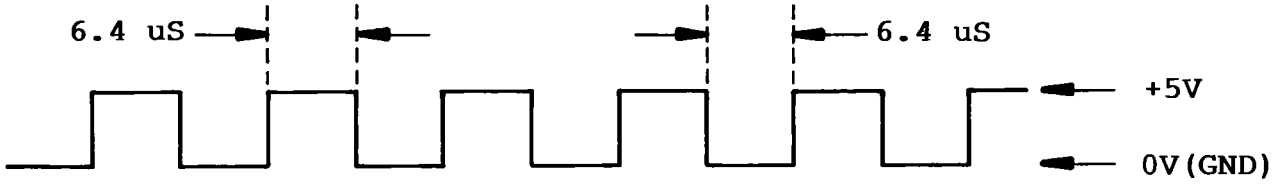
UF4, pin 7 FREQUENCY=78.125 kHz

Figure 8-10.



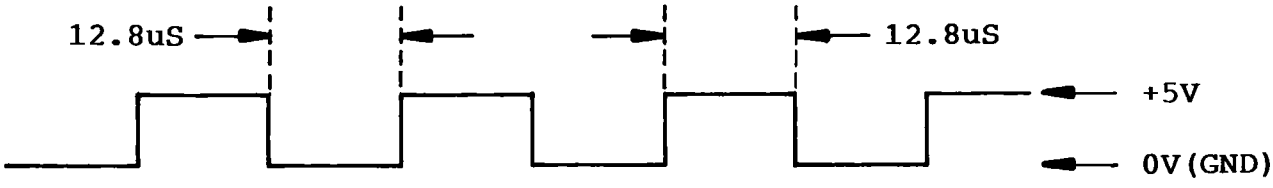
UE3,pin 3 FREQUENCY=156.25 kHz

Figure 8-11.



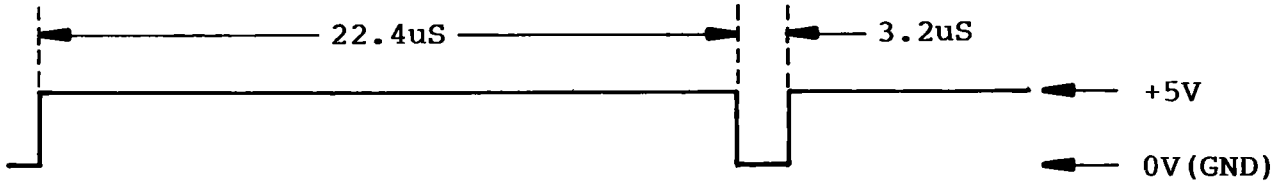
UE3,pin 2 FREQUENCY=78.125 kHz

Figure 8-12.



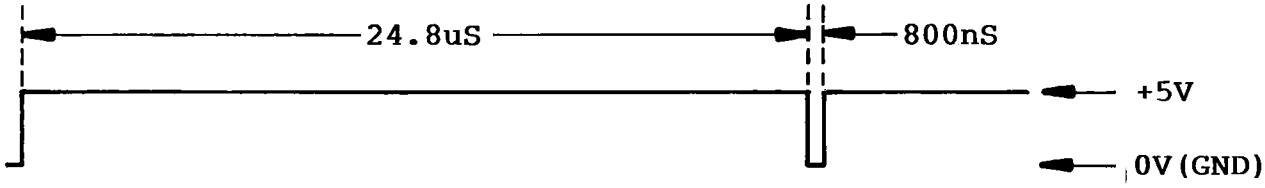
UE3,pin 6 FREQUENCY=39.0625 kHz

Figure 8-13.



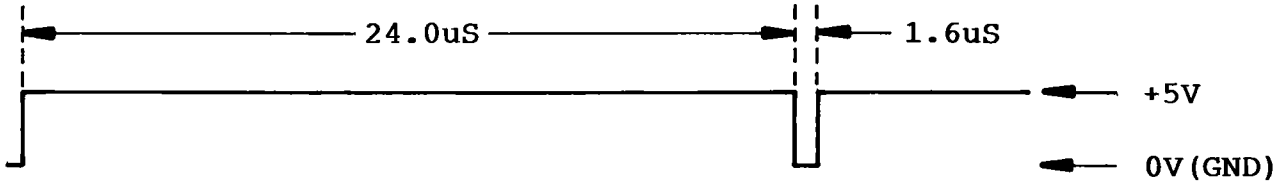
UF3,pin 12 FREQUENCY=39.0625 kHz

Figure 8-14.



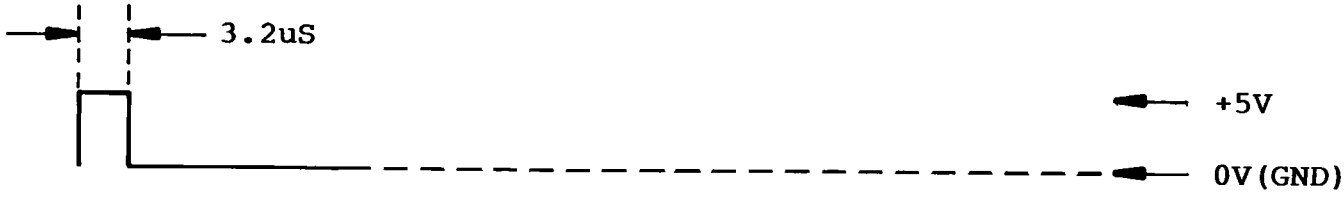
UF3,pin 6 FREQUENCY=39.0625 kHz

Figure 8-15.



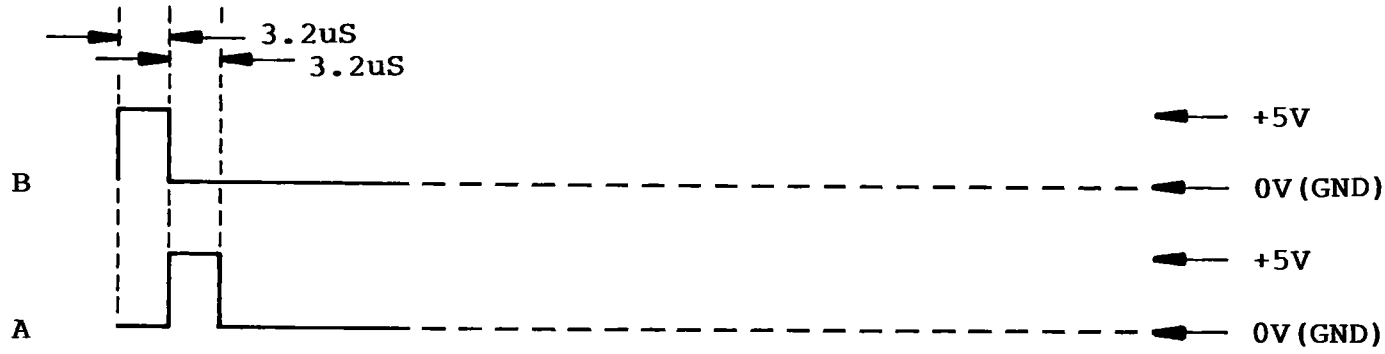
UF3,pin 8 FREQUENCY=39.0625 kHz

Figure 8-16.



UD2,pin 2 Random Pulses

Figure 8-17.



Random Pulses

Step	Connect oscilloscope to following test points: Ch. B	Ch. A	Display
1	UD2,pin3	UD2,pin4	See Above
2	UD2,pin4	UD2,pin5	
3	UD2,pin5	UD2,pin6	
4	UD2,pin6	UD2,pin10	
5	UD2,pin10	UD2,pin11	
6	UD2,pin11	UD2,pin12	
7	UD2,pin12	UD2,pin13	
8	UD2,pin13	UE4,pin5	
9	UE4,pin5	UE4,pin9	

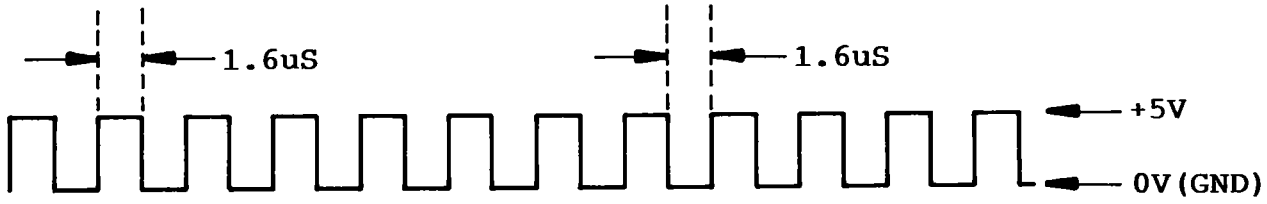
NOTE

Use + trigger and trigger on channel B.

Figure 8-18.

UD3,pin 9 Random Pulses

Figure 8-19.

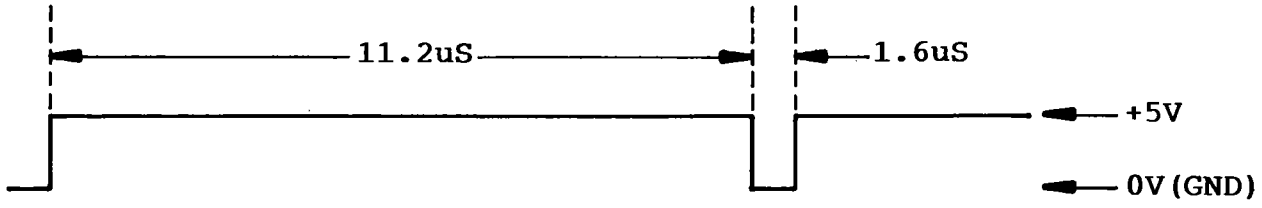


UF5,pin 5 FREQUENCY=312.50 kHz

NOTE

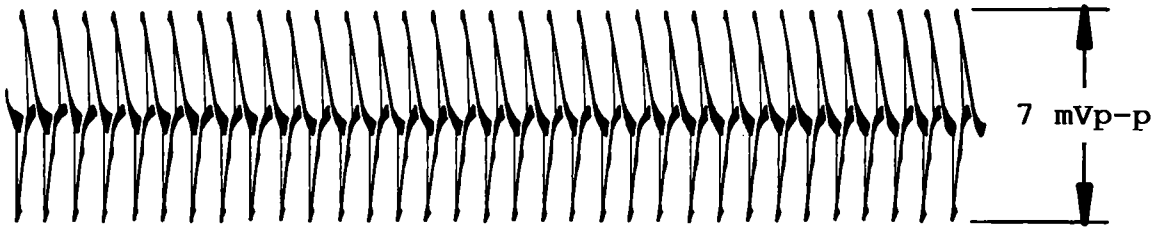
- Signal at UF5, pin 5 is 180^{O} out of phase with signal at UF4, pin 2.

Figure 8-20.

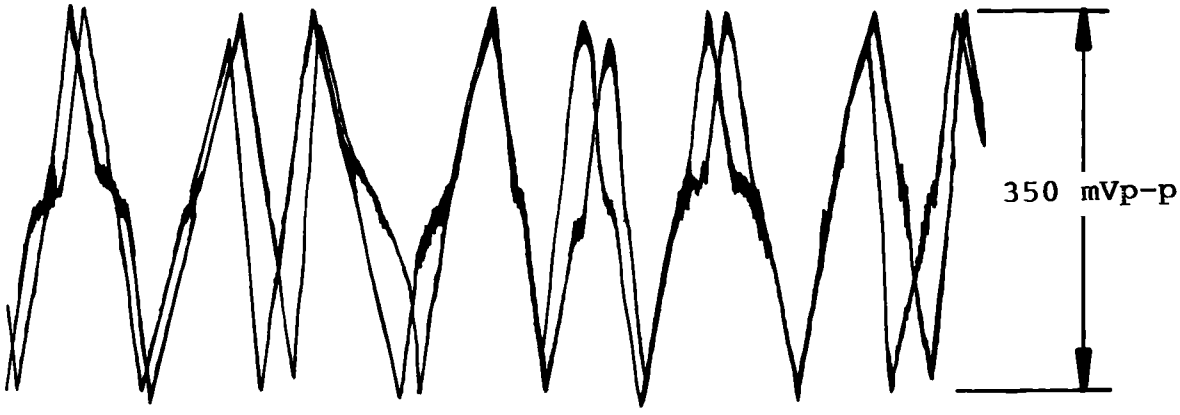


UF5,pin 6 FREQUENCY=78.125 kHz

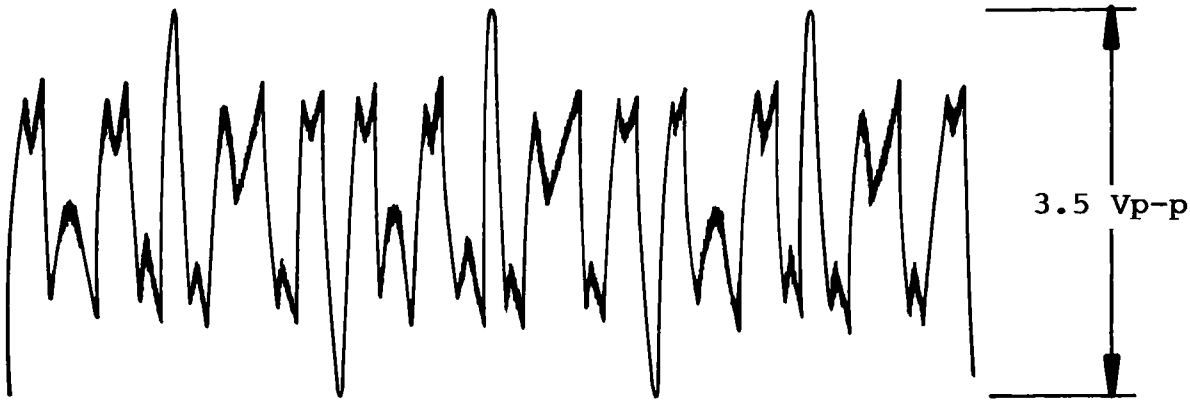
Figure 8-21.



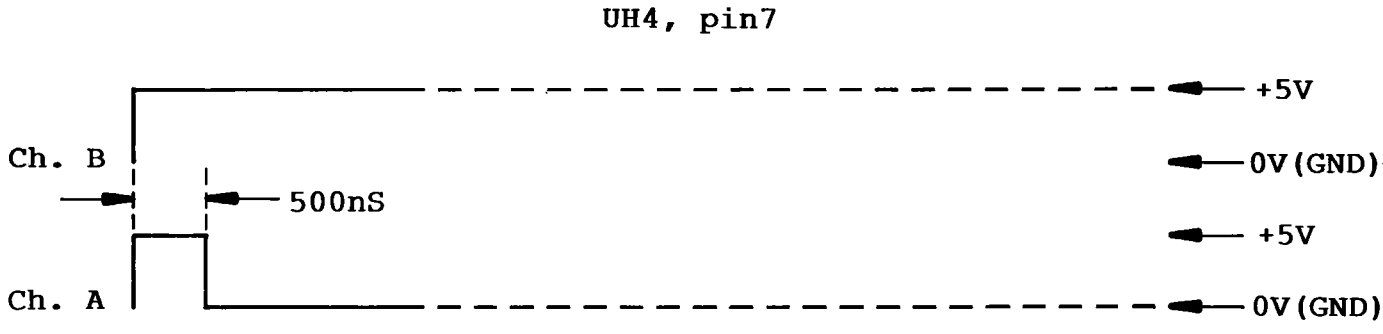
INPUT FROM HEADS
Figure 8-22.



UH7, pins 7 and 8
Figure 8-23.



UH5, pins 7 and 8
Figure 8-24.

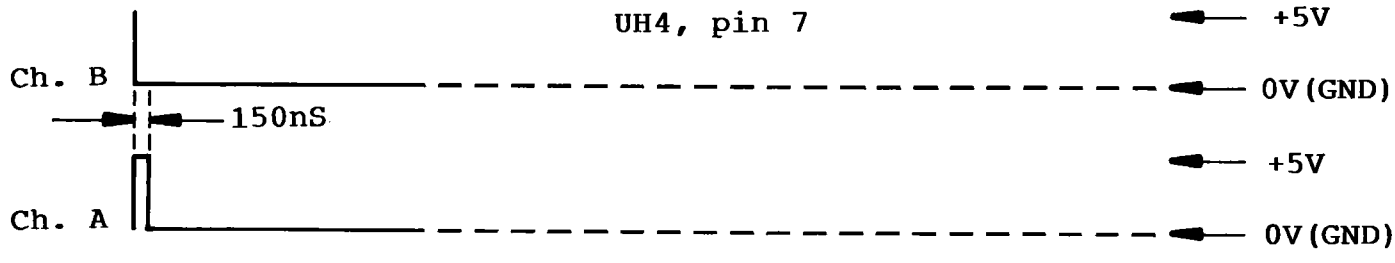


UG2,pin 11 Random Pulses

NOTE

- Trigger on channel B and use + trigger.

Figure 8-25.



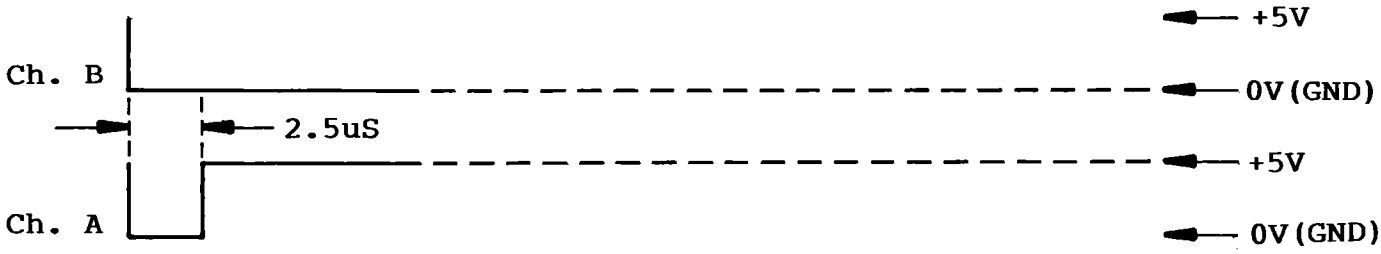
UG2,pin 11 Random Pulses

NOTE

- Trigger on channel B and use - trigger.

Figure 8-26.

UH4,pin 7



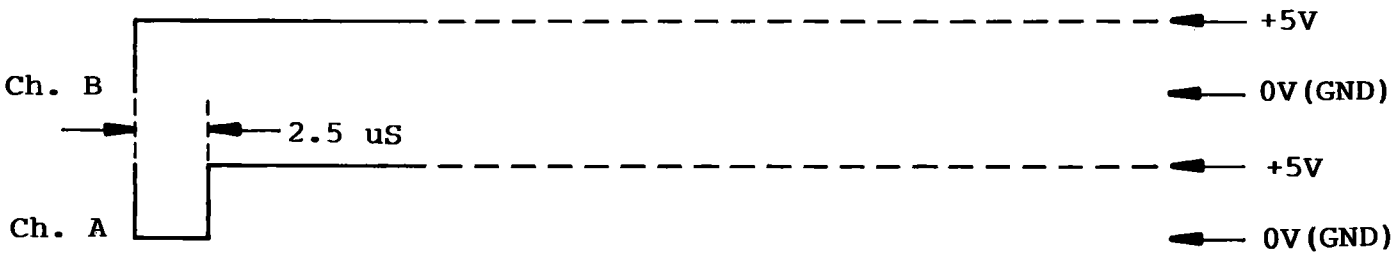
UF6,pin 3 Random Pulses

NOTE

- Trigger on channel B and use - trigger.

Figure 8-27.

UH4,pin7



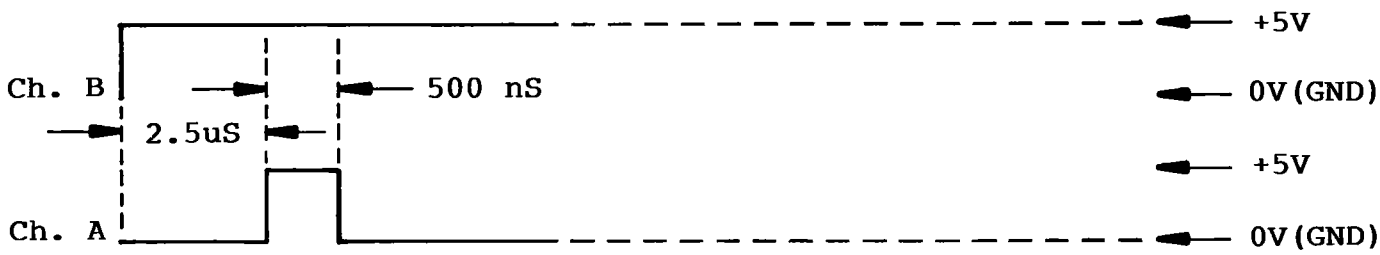
UH6,pin 3 Random Pulses

NOTE

- Trigger on channel B and use + trigger.

Figure 8-28.

UH4,pin 7



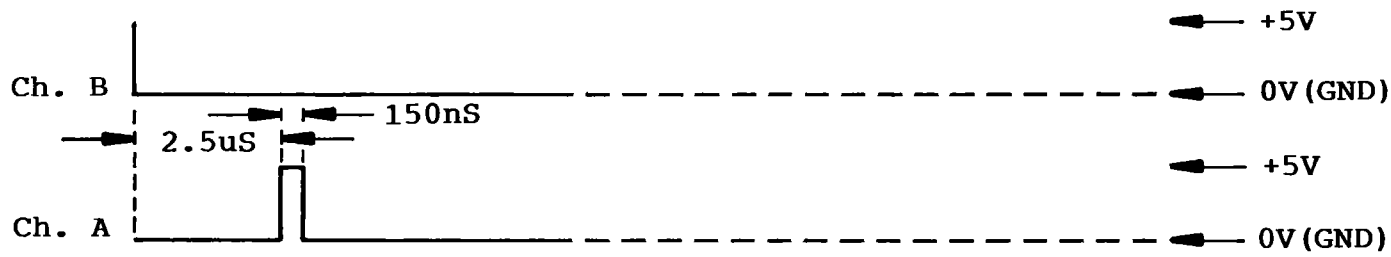
UG2,pin 3 Random Pulses

NOTE

- Trigger on channel B and use + trigger.

Figure 8-29.

UH4,pin 7



UG2,pin 3 Random Pulses

NOTE

- Trigger on channel B and use - trigger.

Figure 8-30.

UH4,pin 7

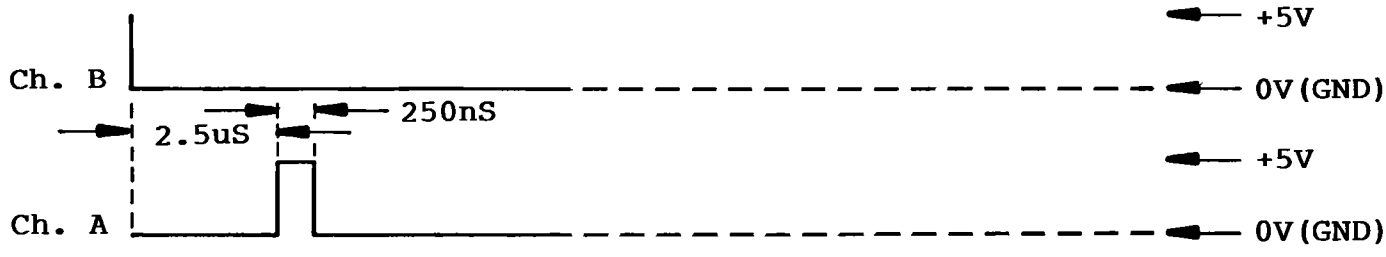
UG3,pin 10 Random Pulses

NOTE

● Trigger on channel B and use + trigger.

Figure 8-31.

UH4,pin 7

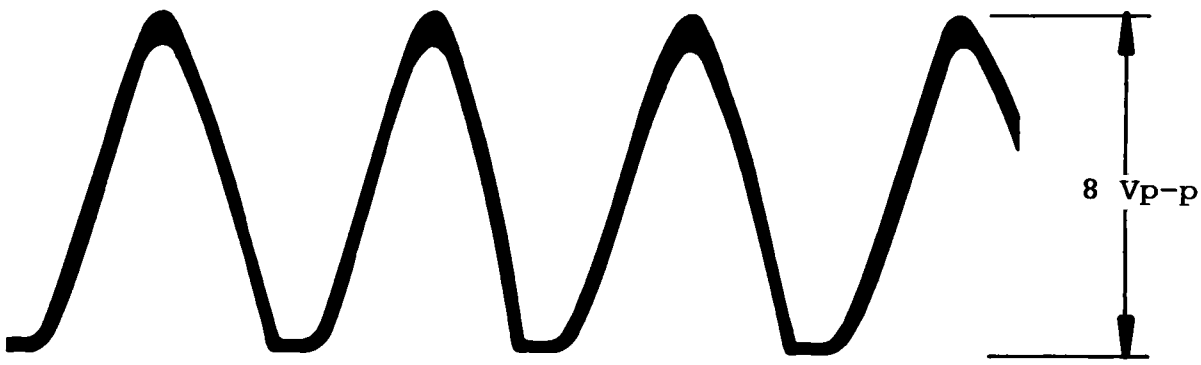


UG3,pin 10 Random Pulses

NOTE

● Trigger on Channel B and use (-) trigger.

Figure 8-32.



OUTPUT OF TACHOMETER (E4 & E5)

Figure 8-33.

SECTION 9
SCHEMATICS
AND
PARTS LAYOUT

Section 9-SCHEMATICS AND PARTS LAYOUTS

9-1. General

This section contains Schematics, Parts Layout Drawings, a Functional Block Diagram and an Interconnect Diagram. These figures are provided for reference purposes. The following index is provided for user convenience:

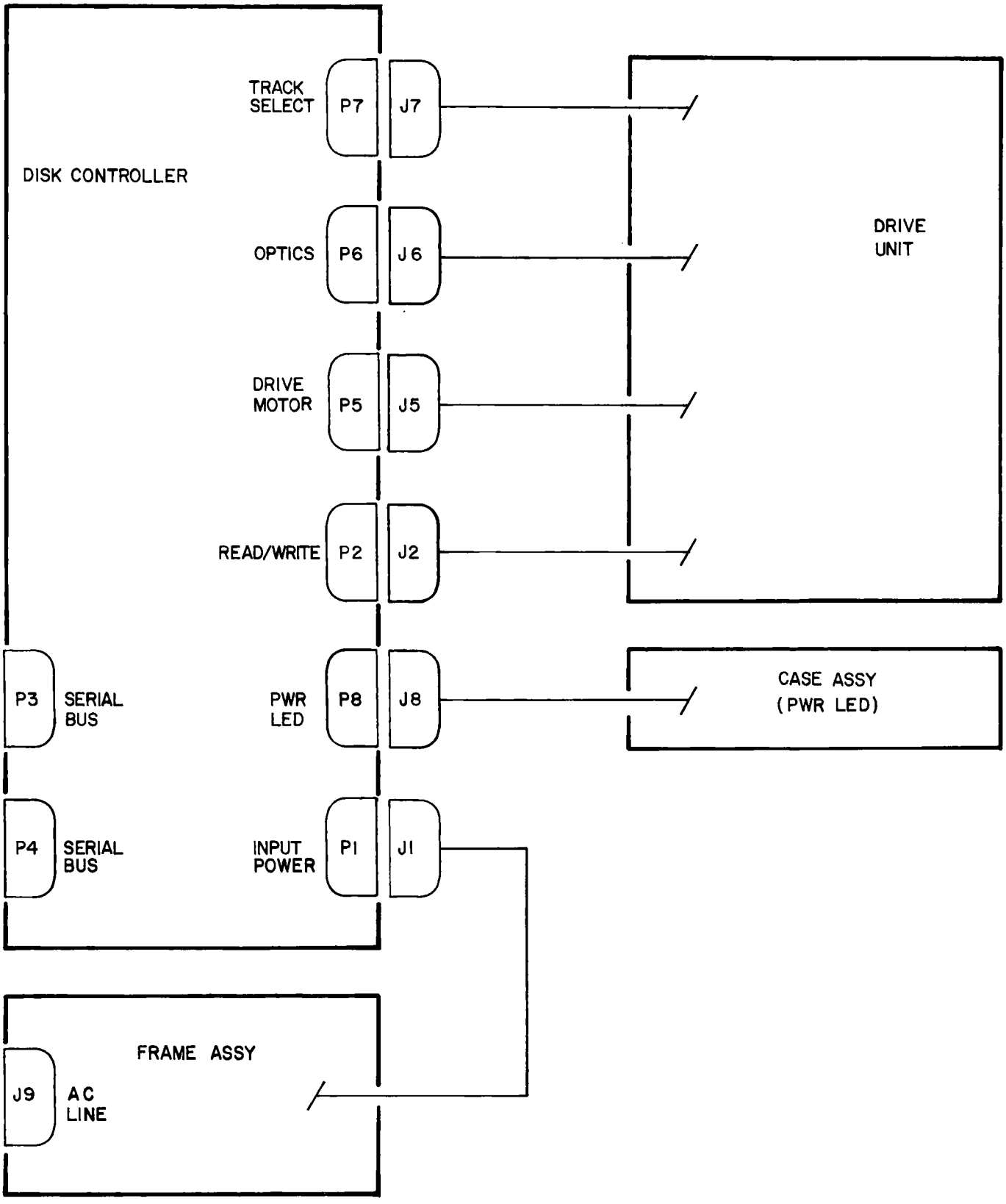


Figure 9-1. Interconnect Diagram

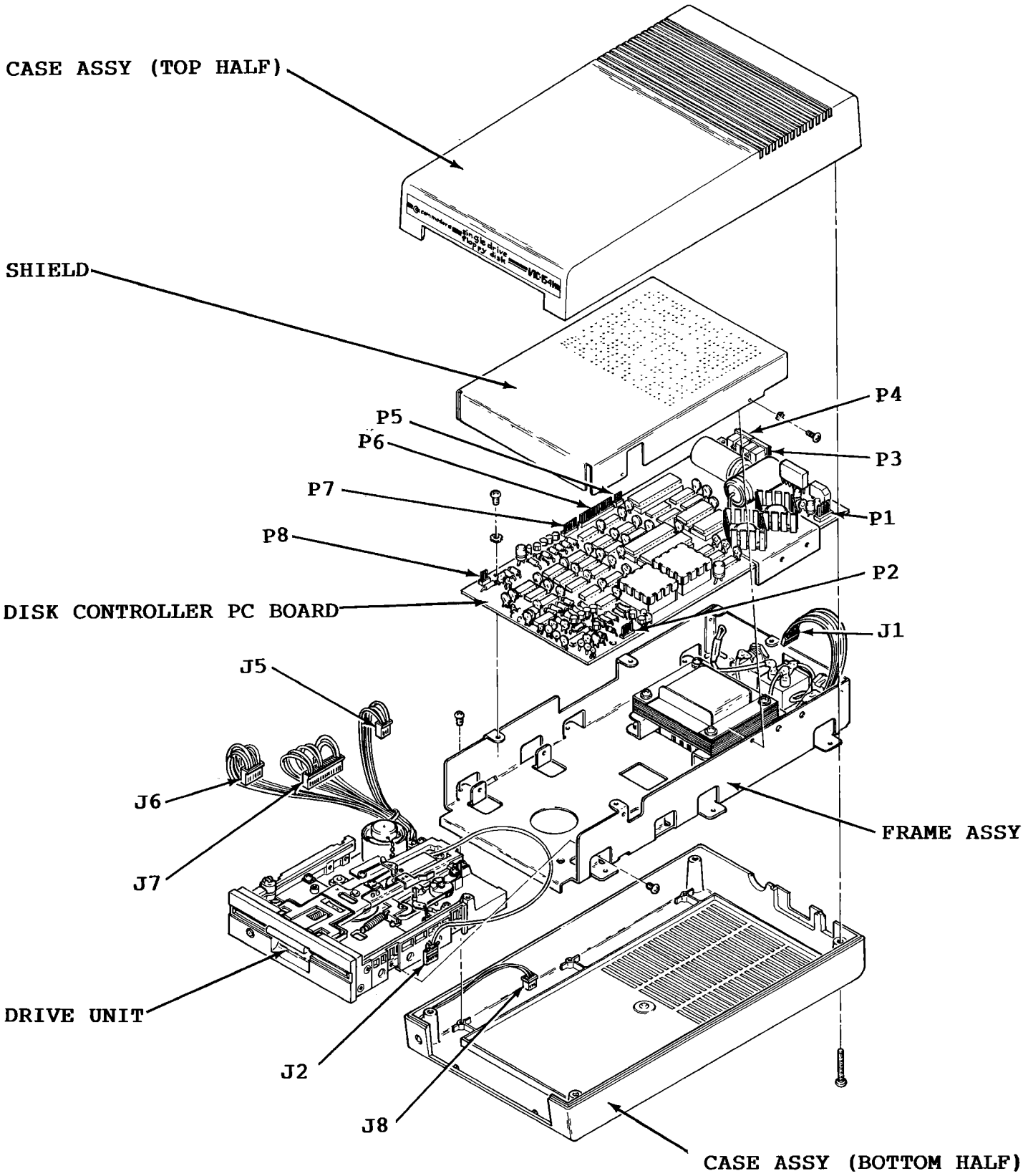


Figure 9-2. Sub-Assembly Identification

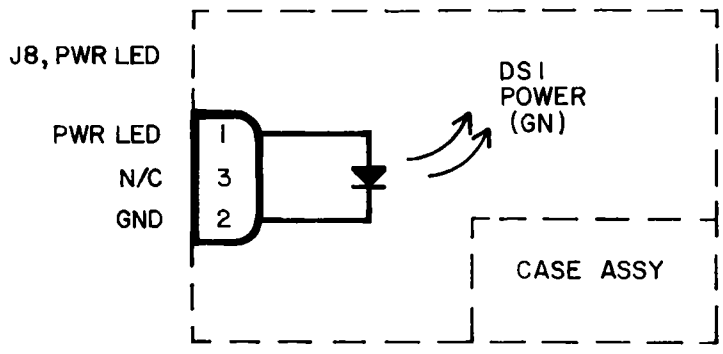


Figure 9-7. Case Assy, Schematic

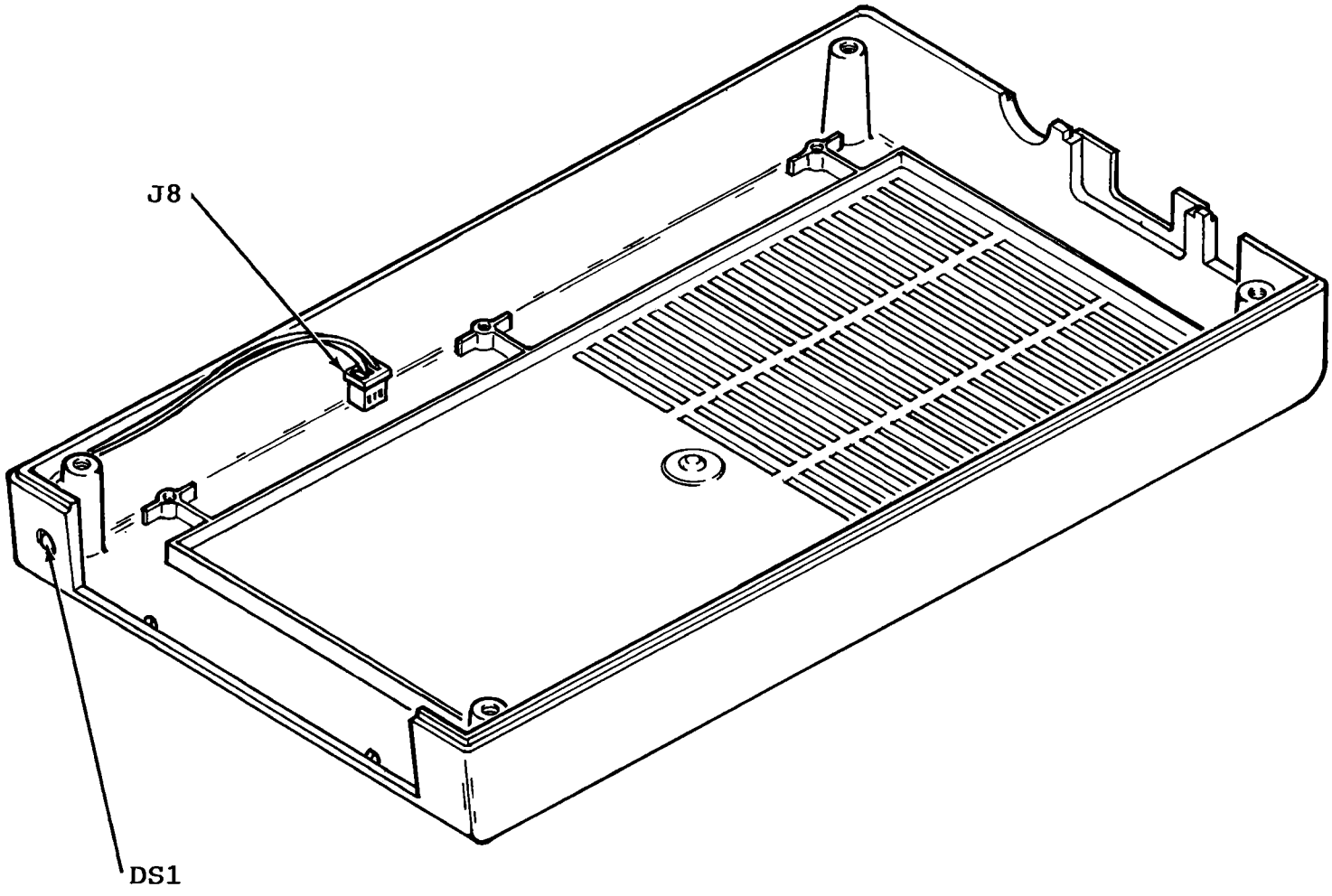


Figure 9-8. Case Assy, Parts Layout

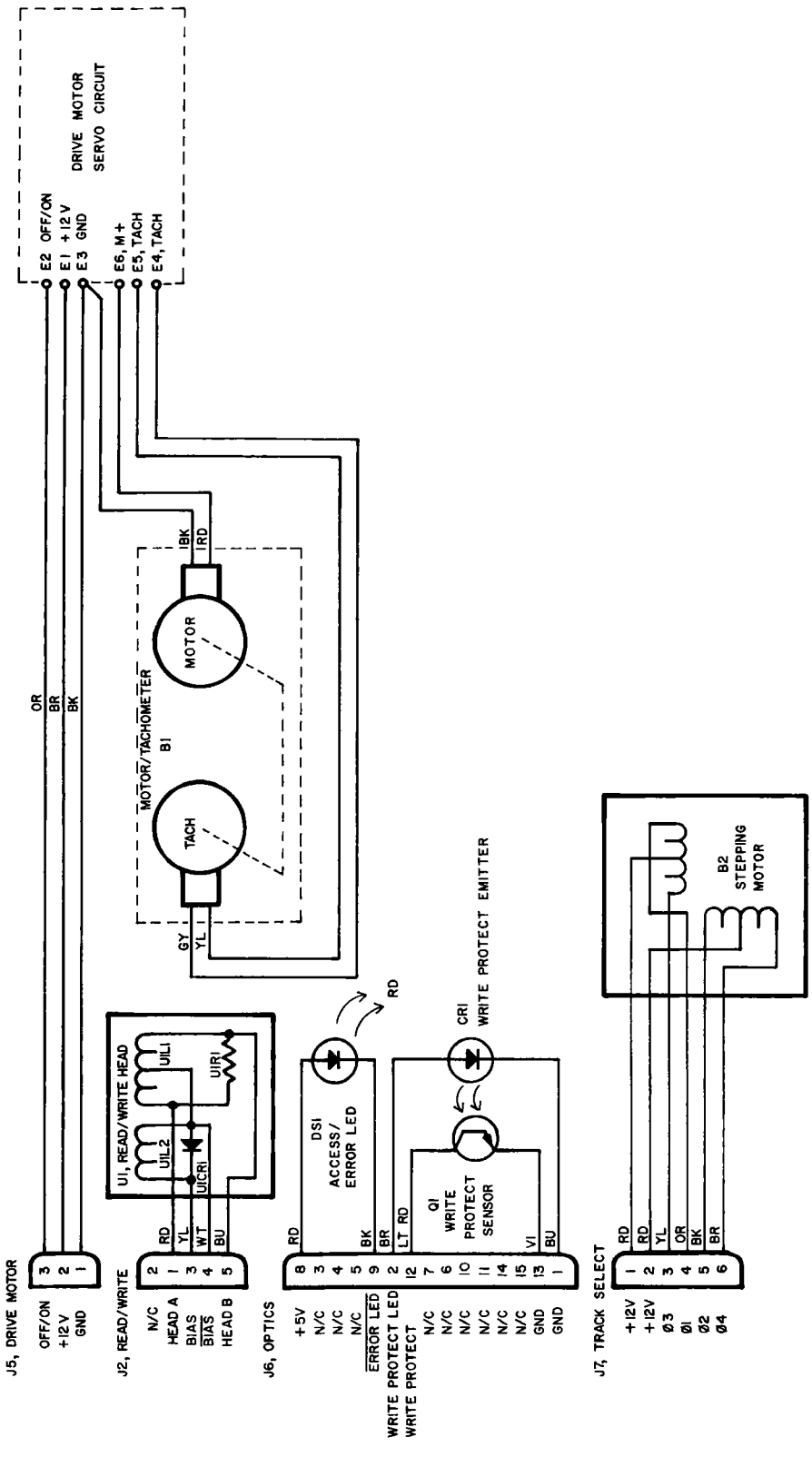


Figure 9-9. Drive Unit, Schematic

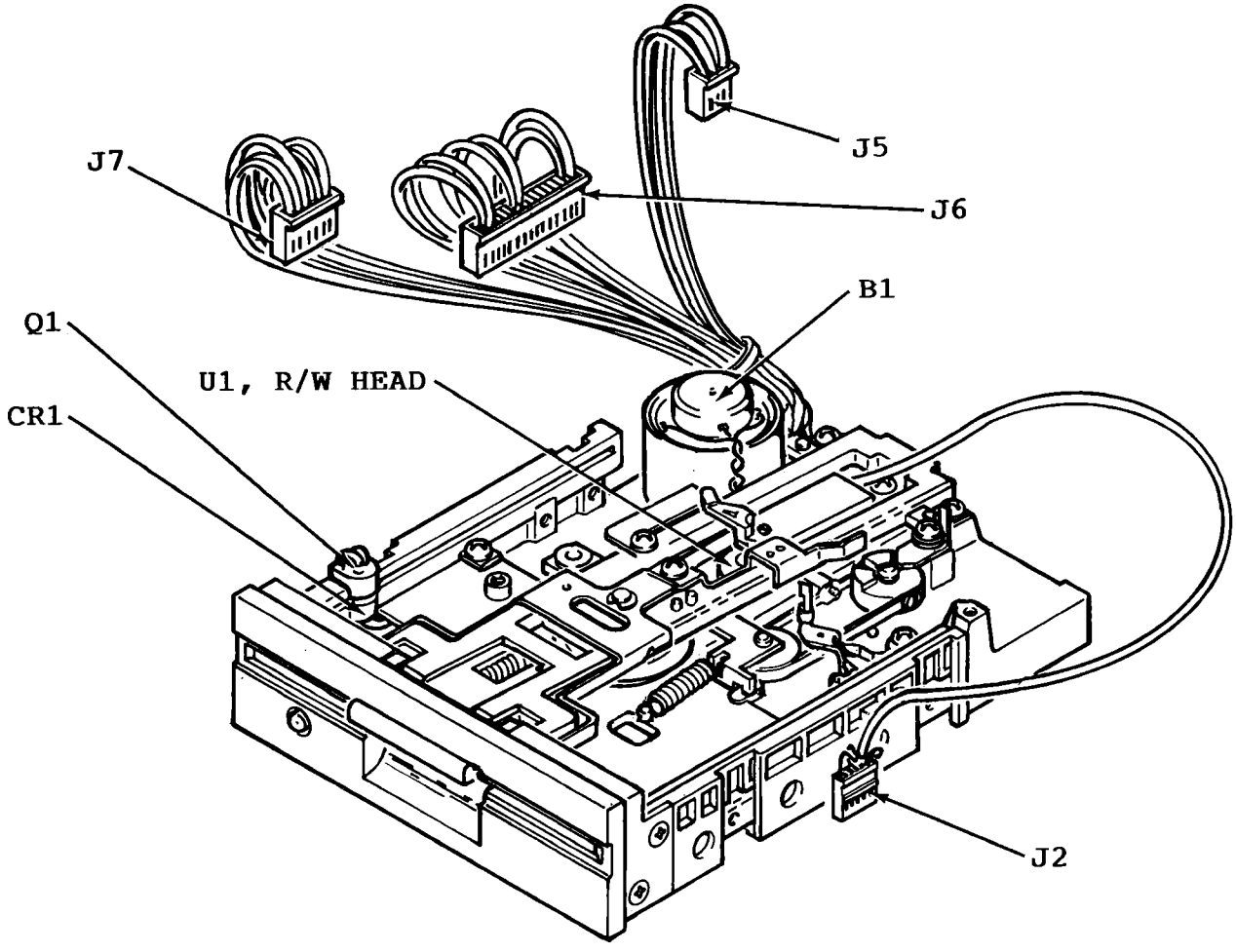


Figure 9-10. Drive Unit, Parts Layout (Top)

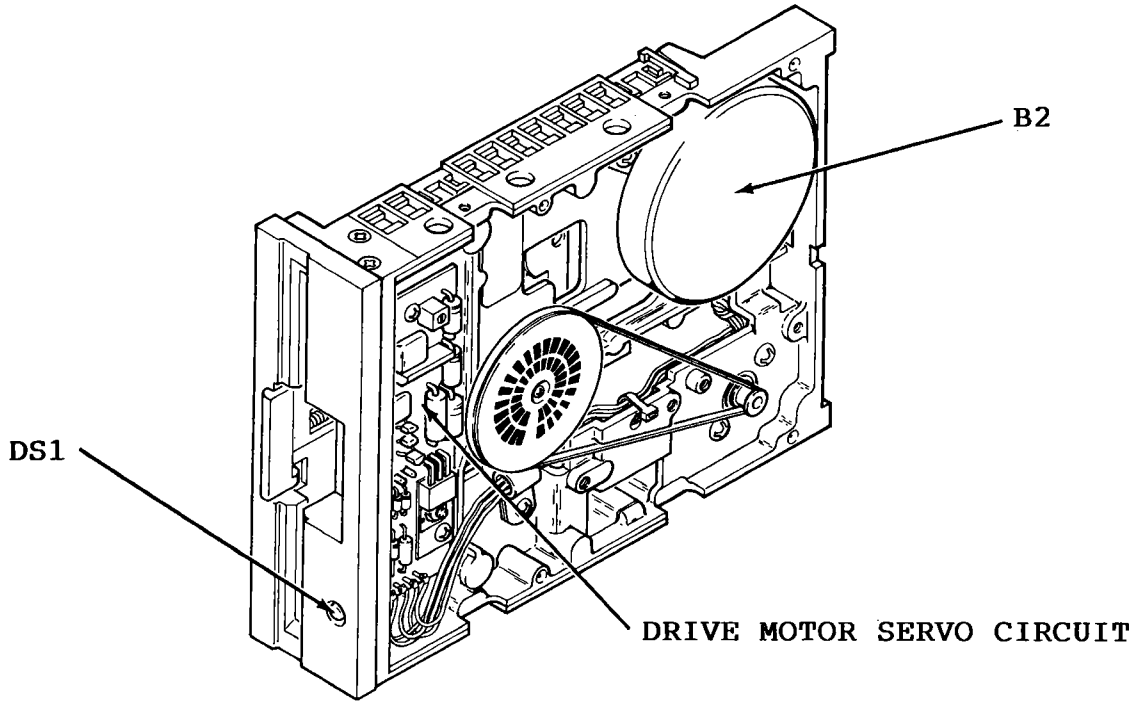


Figure 9-11. Drive Unit, Parts Layout (Bottom)

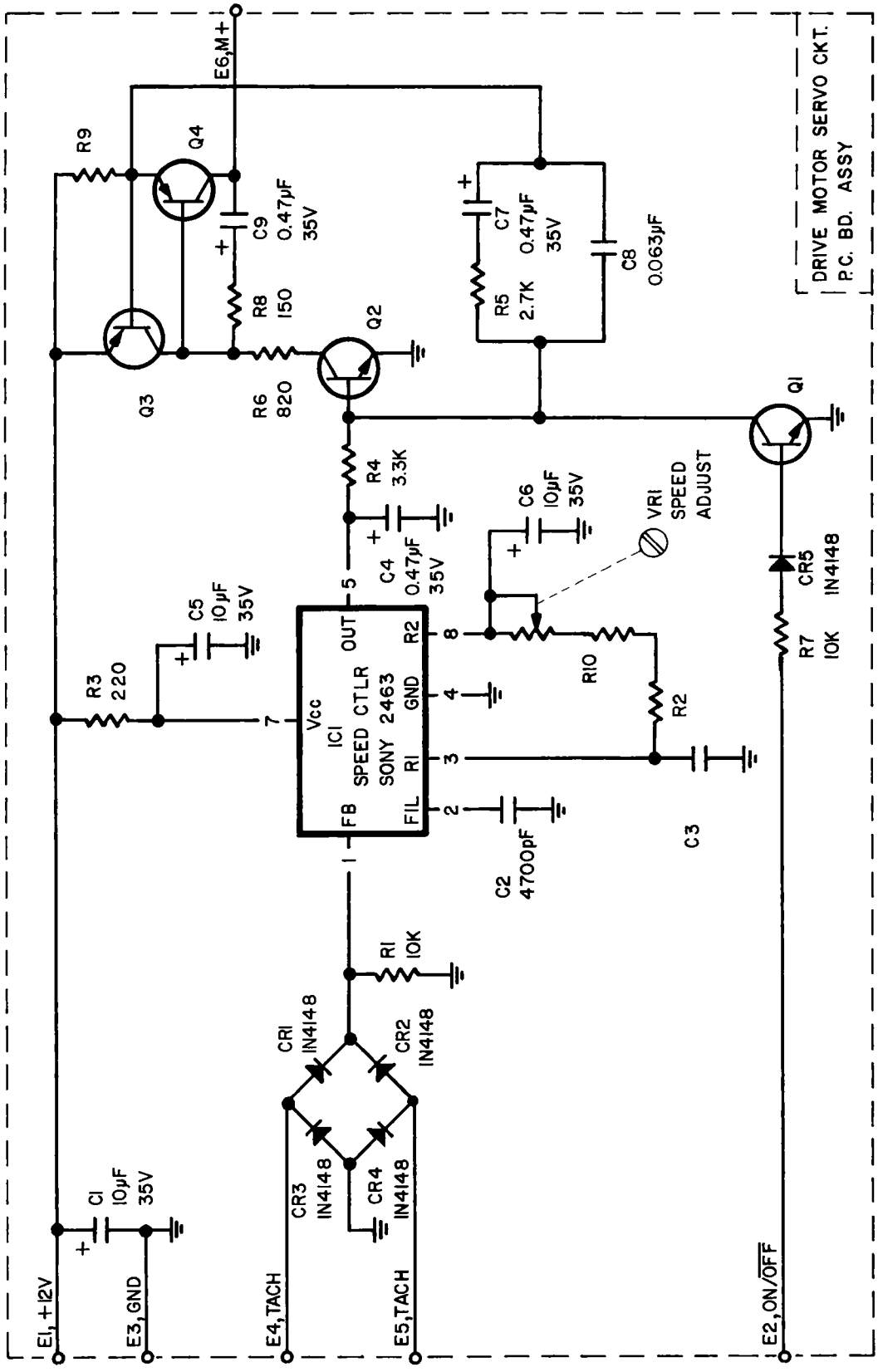


Figure 9-12. Drive Servo Circuit, Schematic

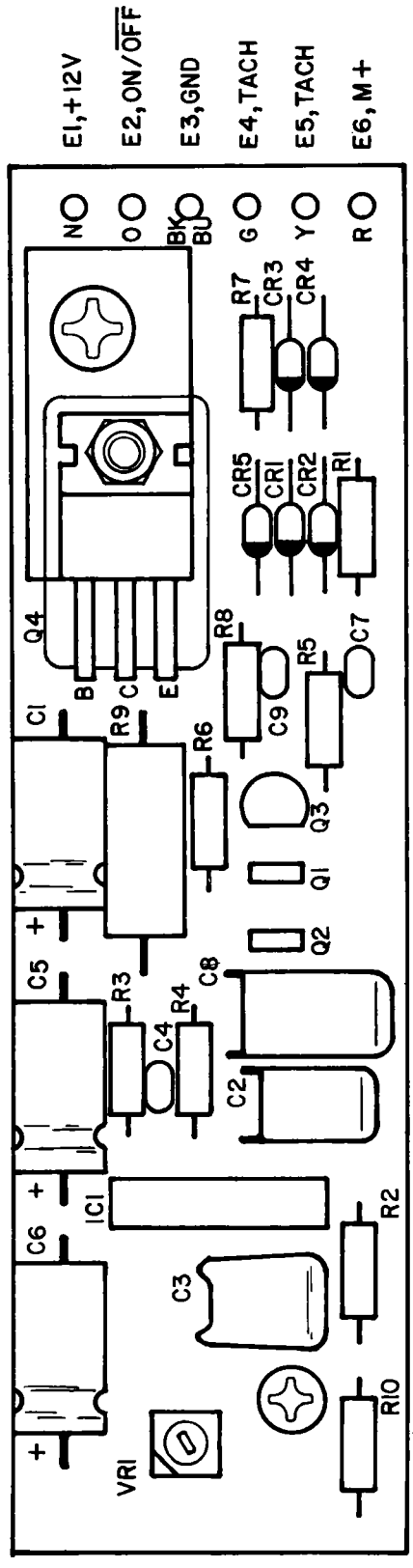


Figure 9-13. Drive Servo Circuit, Parts Layout

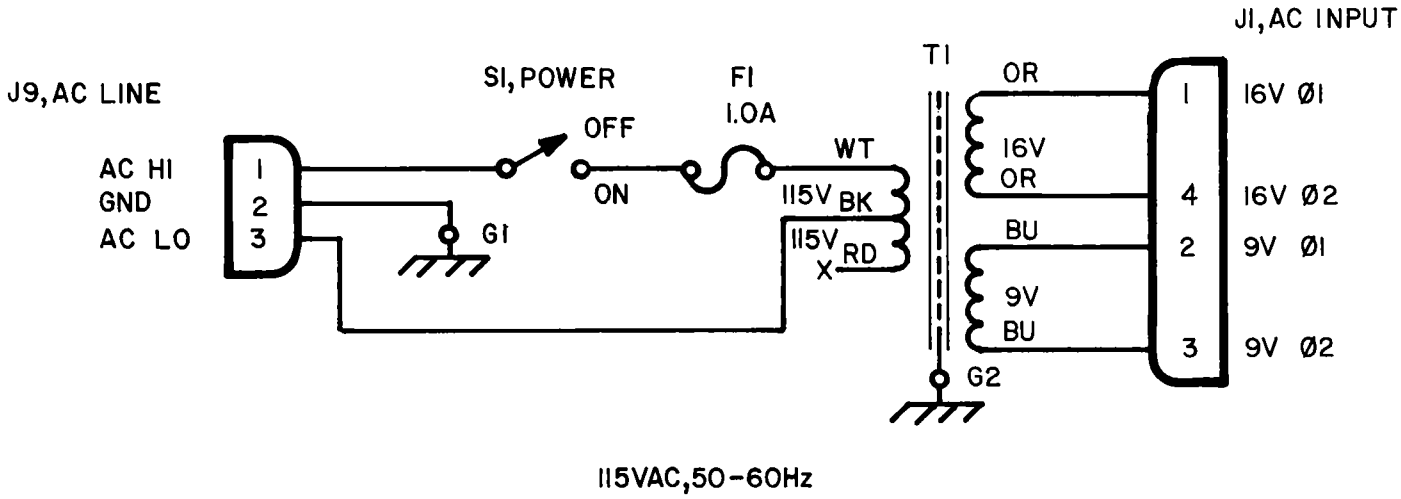


Figure 9-14. Frame Assy, Schematic (115 VAC)

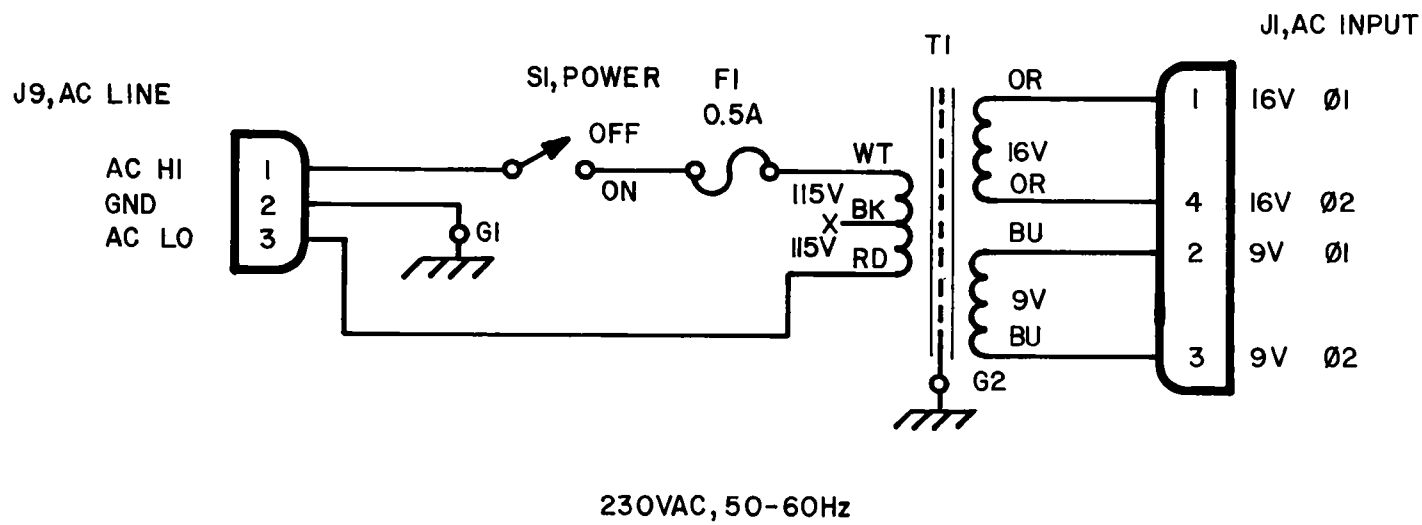


Figure 9-15. Frame Assy, Schematic (230 VAC)

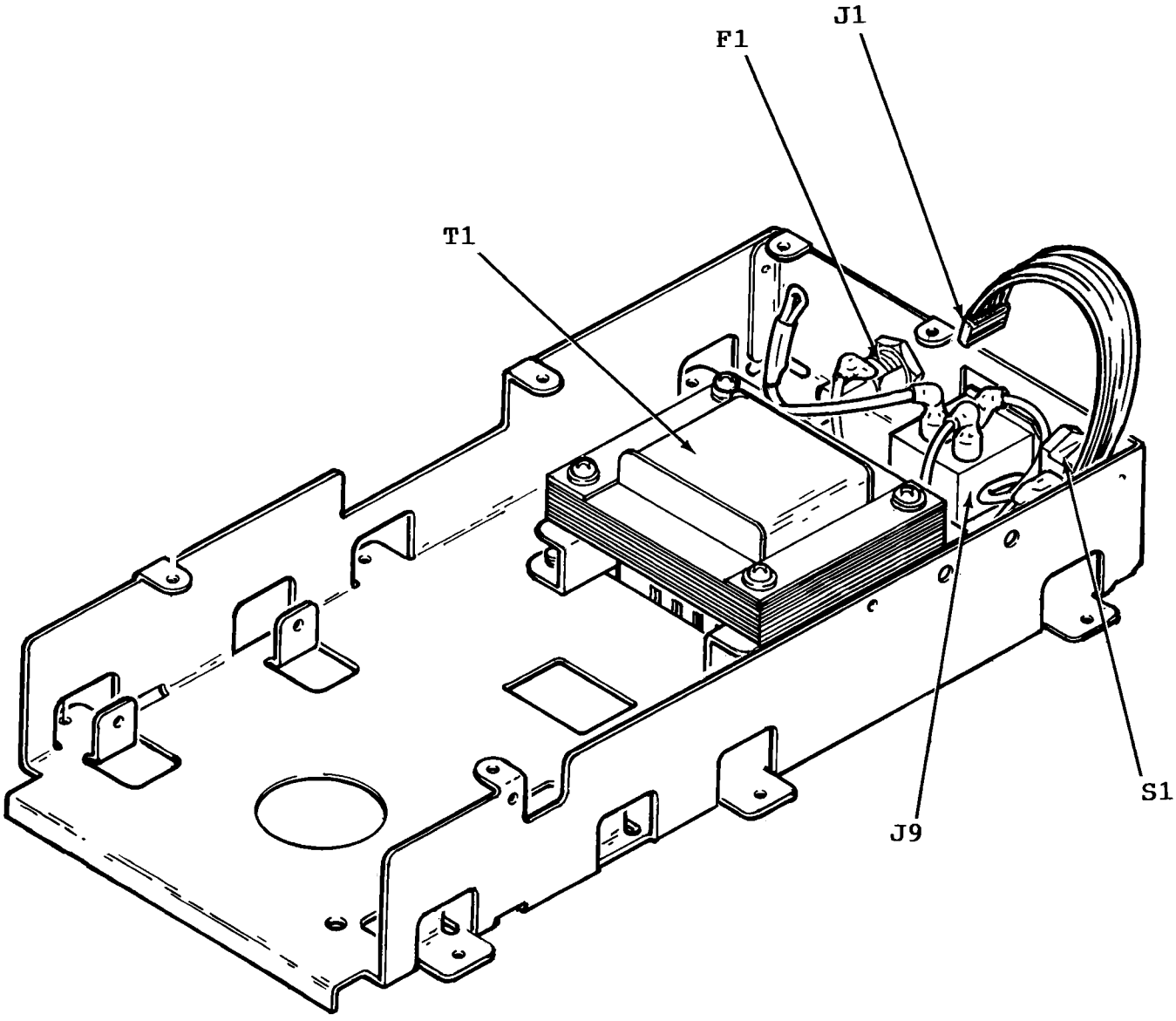


Figure 9-16. Frame Assy, Parts Layout

APPENDIX A

APPENDIX A

Test Equipment Specifications

This appendix contains the recommended specifications for test equipment used in servicing the VIC-1541.

Digital Multi-Meter	Display-3 1/2 digit Accuracy-2 per cent full scale Sensitivity- 100 KOhm/Volt Ranges DC Volts-9 to +30 V AC Volts-0 to 250 Vrms Ohms-0 ohms to infinity Resolution DC Volts-0.01 V AC Volts-1.0 V Ohms-1.0 Ohms
Oscilloscope	Display-Dual trace Input impedance-1 Mohm,15pF Vert sens-to 5 V/Div Input coupling-AC 6 DC Vert Bandwidth-DC to 30 MHz(50 MHz preferred) Time base-100nS/Div to 10mS/Div Trigger sources-CH B & Line Trigger modes-(+) trigger & (-) trigger
Frequency Counter	Accuracy-2% Range-39 KHz to 16 MHz Resolution-10 Hz
Timing Strobe	See Appendix B

APPENDIX B

APPENDIX B

Fabrication of Timing Light

Materials Required:

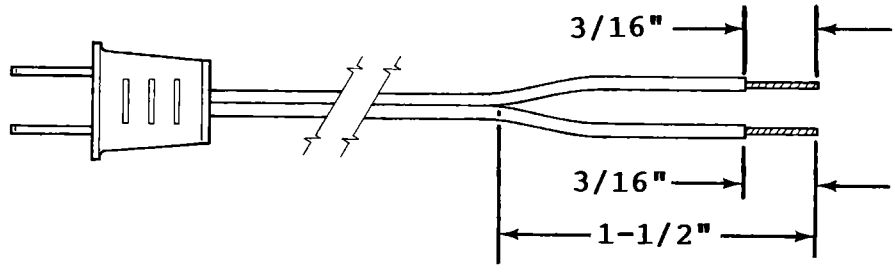
One neon bulb
One lamp cord with appropriate plug
One resistor 22K,10%,1/4 W (for 115 VAC)
47K,10%,1/4 W (for 220 VAC)

Equipment and Supplies:

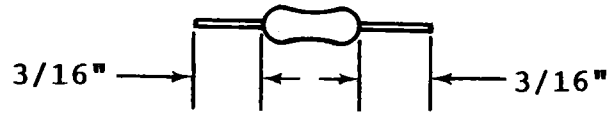
Knife
Soldering iron
Wire cutters
Needle nose pliers
Heat shrink tubing, 1/8 inch
Heat shrink tubing, 3/16 inch
Solder, 60/40 resin core
Scale (ruler)
Ohmmeter

Preparation:

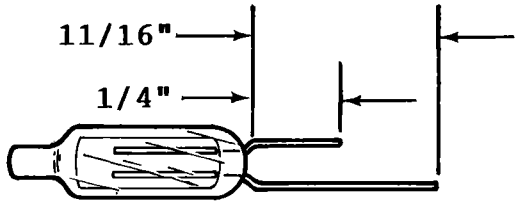
1. Prepare lamp cord as shown below:



2. Prepare resistor as shown below:



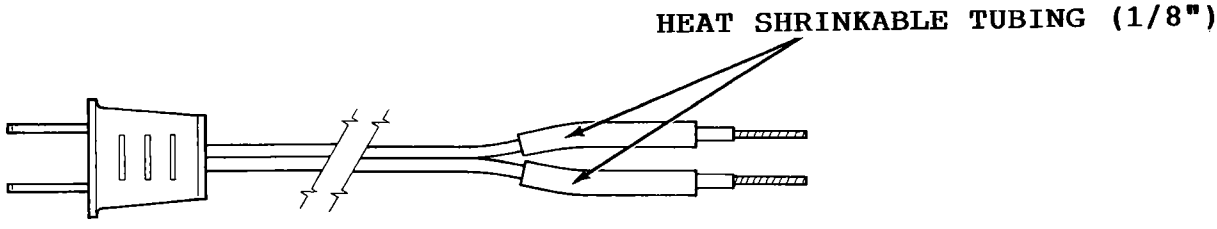
3. Prepare neon lamp as shown below:



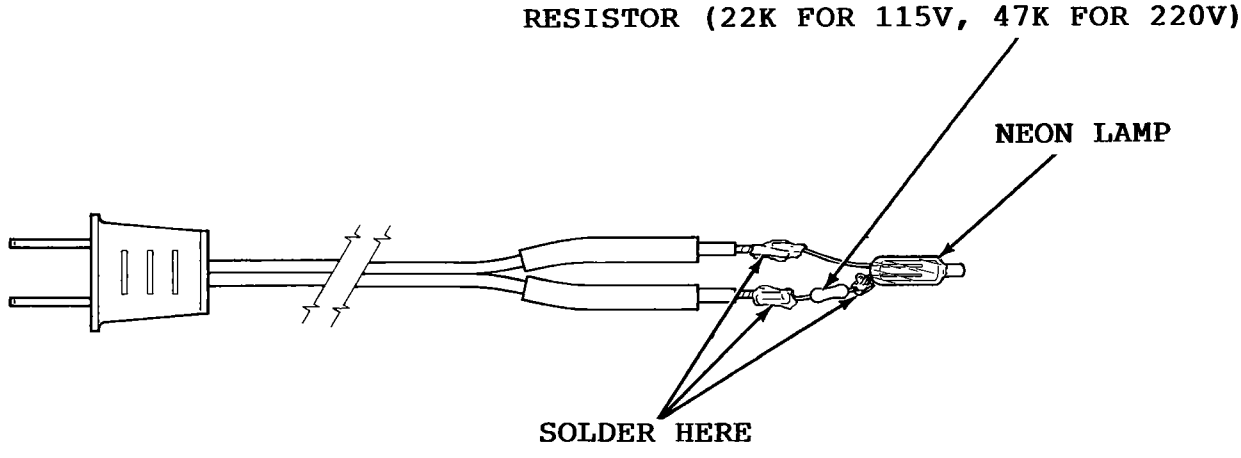
4. Tin all leads on lamp cord, resistor and neon lamp.

Assembly:

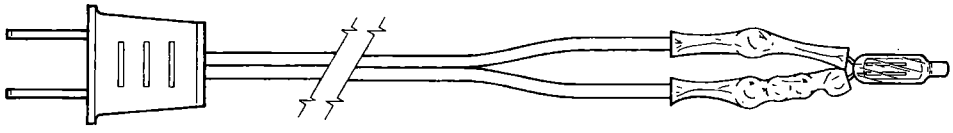
1. Slide 1 inch lengths of 1/8 inch heat shrink tubing onto each of the prepared leads of the lamp cord. Do not shrink the tubing at this time.



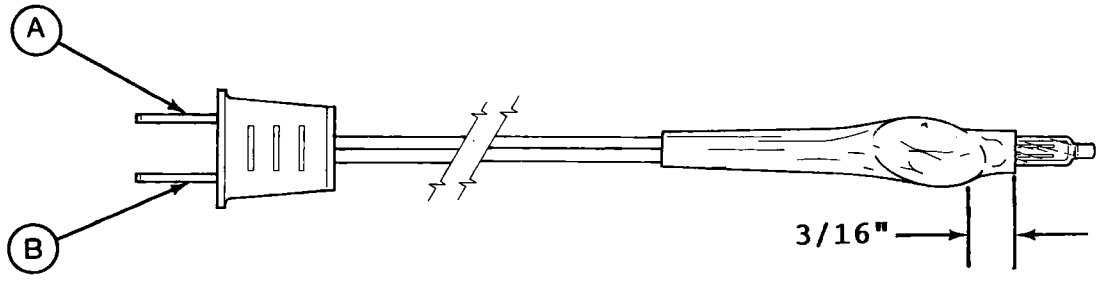
2. Solder components as shown below. Either lead of the line cord may be soldered to the resistor as long as the other lead is soldered to the neon lamp.



3. Slide both pieces of heat shrink tubing toward the base of the neon lamp and then shrink the tubing.



4. Slide a 2 inch length of 3/16 inch heat shrink tubing over neon lamp. Position the end of the heat shrink tubing 3/16 inch up from the base of the neon lamp and then shrink the tubing.



WARNING

- BEFORE PLUGGING IN TIMING LIGHT, USE OHMMETER TO VERIFY RESISTANCE BETWEEN POINTS A AND B IS INFINITY.

APPENDIX C

APPENDIX C

MOS Handling Precautions

When handling the controller board or any of the MOS IC's used in the VIC-1541, the technician must be aware of possible damage to the MOS IC's from static discharge.

A static charge of only several hundred volts is enough to cause permanent damage to a MOS IC. It is not uncommon for the human body to accumulate tens of thousands of volts of static charge. The following precautions will help to reduce damage caused by static charges:

Avoid wearing synthetic material when servicing the VIC-1541.

Do not service the VIC-1541 in a room with carpeting on the floor.

The use of conductive floor mats and wrist straps is advised (if possible).

Before handling PC Board, touch a ground such as a shop ground or a cold water pipe for 30-60 seconds to discharge any static charge in your body. Also touch any tools being used or anti-static devices (i.e., conductive foam rubber or conductive packaging tubes) to the same ground.

Avoid touching the pins of IC's as much as possible.

After removing a MOS IC for troubleshooting purposes, place IC into conductive foam until reinstalled.

When replacing MOS IC's, always ground conductive packaging to shop ground or cold water pipe before handling the IC.

APPENDIX D

APPENDIX D

Parts List

Disk Controller PC Board

Designator	Description	Value/Part number
C1	Capacitor	1uF,50V
C2	Capacitor	47uF,16V
C3	Capacitor	0.1uF
C4	Capacitor	1uF,50V
C5	Capacitor	47uF,16V
C6	Capacitor	0.1uF
C7	Capacitor	0.1uF
C8	Capacitor	0.1uF
C9	Capacitor	0.1uF
C10	Capacitor	68pF
C11	Capacitor	0.1uF
C12	Capacitor	10uF,25V
C13	Capacitor	0.1uF
C14	Capacitor	0.1uF
C15	Capacitor	0.47uF,35V
C16	Capacitor	680pF
C17	Capacitor	0.1uF
C18	Capacitor	0.1uF
C19	Capacitor	0.1uF
C20	Capacitor	0.1uF
C21	Capacitor	0.1uF
C22	Capacitor	0.1uF
C23	Capacitor	3.3uF,25V
C24	Capacitor	0.47uF,35V
C25	Capacitor	0.1uF
C26	Capacitor	1000pF
C27	Capacitor	680pF
C28	Capacitor	330pF
C29	Capacitor	0.1uF
C30	Capacitor	0.1uF
C31	Capacitor	0.1uF
C32	Capacitor	0.1uF
C33	Capacitor	150pF
C34	Capacitor	0.1uF
C35	Capacitor	0.1uF
C36	Capacitor	0.1uF
C37	Capacitor	0.1uF
C38	Capacitor	0.1uF
C39	Capacitor	0.1uF
C40	Capacitor	0.1uF
C41	Capacitor	0.1uF
C42	Capacitor	0.1uF
C43	Capacitor	0.1uF
C44	Capacitor	0.1uF
C45	Capacitor	0.1uF

Designator	Description	Value/Part number
C46	Capacitor	0.1uF
C47	Capacitor	0.1uF
C48	Capacitor	0.1uF
C49	Capacitor	330pF
C50	Capacitor	680pF
C51	Capacitor	6800uF,25V
C52	Capacitor	10,000uF,16V
C53	Capacitor	0.1uF
C54	Capacitor	0.1uF
C55	Capacitor	0.1uF
C56	Capacitor	100uF,15V
C57	Capacitor	0.1uF
C58	Capacitor	.022uF
C59	Capacitor	.022uF
C60	Capacitor	0.1uF
C61	Capacitor	0.1uF
C62	Capacitor	4.7uF
C63	Capacitor	1.0uF
C64	Capacitor	0.1uF
C65	Capacitor	220uF,10V
CR1	Bridge Rectifier	8241
CR2	Diode	1N4002
CR3	Bridge Rectifier	8240
CR4	Diode	1N4002
CR5	Zener Diode	3.3V
CR6	Diode	1N4148
CR7	Diode	1N4148
CR8	Diode	1N4148
CR9	Diode	1N4148
CR10	Diode	1N4148
CR11	Diode	1N4148
CR12	Diode	------
CR13	Diode	1N4002
CR14	Diode	1N4002
CR15	Diode	1N4002
CR16	Diode	1N4002
CR17	Diode	1N4002
L1	Inductor	
L2	Inductor	
L3	Inductor	
L4	Inductor	
L5	Inductor	Values
L6	Inductor	Not
L7	Inductor	Available
L8	Inductor	
L9	Inductor	
L10	Inductor	
L11	Inductor	
L12	Inductor	

Designator	Description	Value/Part number
L13	Inductor	Values Not Available
L14	Inductor	
L15	Inductor	
L16	Inductor	
Q1	Transistor	2SA952
Q2	Transistor	2SC945
Q3	Transistor	2SC945
Q4	Transistor	2SC2001
Q5	Transistor	2SC2001
Q6	Transistor	2SC2001
Q7	Transistor	2SC2001
Q8	Transistor	2SA1015
Q9	Transistor	2SA1015
Q10	Transistor	2SA1015
Q11	Transistor	2SA1015
R1	Resistor,1/4W	330
R2	Resistor,1/4W	330
R3	Resistor,1/4W	47
R4	Not Used	
R5	Resistor,1/4W	330
R6	Resistor,1/4W	1.0K
R7	Resistor,1/4W	22K
R8	Resistor,1/4W	---
R9	Resistor,1/4W	680
R10	Resistor,1/4W	22K
R11	Resistor,1/4W	1.0K
R12	Resistor,1/4W	9.10K
R13	Resistor,1/4W	9.10K
R14	Resistor,1/4W	2.2K
R15	Resistor,1/4W	2.2K
R16	Resistor,1/4W	220
R17	Resistor,1/4W	200
R18	Resistor,1/4W	150
R19	Resistor,1/4W	150
R20	Resistor,1/4W	330
R21	Resistor,1/4W	3.0
R22	Resistor,1/4W	3.0
R23	Resistor,1/4W	3.0
R24	Resistor,1/4W	510
R25	Resistor,1/4W	360
R26	Resistor,1/4W	2.2K
R27	Resistor,1/4W	470
R28	Resistor,1/4W	470
R29	Resistor,1/4W	22K
R30	Resistor,1/4W	360
R31	Resistor,1/4W	1.0K
R32	Resistor,1/4W	1.0K
R33	Resistor,1/4W	1.0K
R34	Resistor,1/4W	1.0K

Designator	Description	Value/Part number
R35	Resistor,1/4W	150
R36	Resistor,1/4W	150
R37	Resistor,1/4W	330
R38	Not Used	
R39	Resistor,1/4W	680
R40	Resistor,1/4W	680
R41	Resistor,1/4W	680
R42	Resistor,1/4W	680
R43	Resistor,1/4W	1.0K
R44	Not Used	
R45	Resistor,1/4W	220
R46	Not Used	
R47	Resistor,1/4W	470
R48	Resistor,1/4W	1.5K
R49	Resistor,1/4W	100
R50	Resistor,1/4W	470
R51	Resistor,1/4W	2.2K
R52	Resistor,1/4W	2.2K
R53	Resistor,1/4W	22K
R54	Resistor,1/4W	150
R55	Resistor,1/4W	470
R56	Resistor,1/4W	2.2K
R57	Resistor,1/4W	470
R58	Resistor,1/4W	1.0K
UA2	1024 x 4 Bit Static RAM	2114L3
UA3	1024 x 4 Bit Static RAM	2114L3
UAB1	Versatile Interface Adapter	6522
UAB4	8K x 8 ROM	235302-01
UAB5	8K x 8 ROM	981229-01
UB2	1024 x 4 Bit Static RAM	2114L3
UB3	1024 x 4 Bit Static RAM	2114L3
UB6	Hex Inverter	74LS04
UB7	Quad 2 input pos. NAND Gate	74LS00
UB8	BCD-to-Decimal Decoder	74LS42
UC1	Hex Schmitt-Trigger Inverter	74LS14
UC2	13 input pos. NAND Gate	74LS133
UC3	Octal Bus Transceiver	74LS245
UC6	Binary Presettable Counter/Latch	74LS197
UC7	Quad 2 input pos. NOR Gate	7402
UCD4	Versatile Interface Adapter	6522
UCD5	8-Bit Microprocessor	6502
UD1	Hex Inverter Buffer/Driver	7406
UD2	8-Bit Parallel Output Serial Shift Register	74LS164
UD3	Parallel Load 8-Bit Shift Register with Complementary Outputs	74LS165
UE2	Dual 2 to 4 Line Decoder/ Multiplexer	74LS139
UE3	Binary Synchronous Up/Down Counter	74LS191
UE4	Dual-D Flip-Flop	74LS74

Designator	Description	Value/Part number
UE5	Quad 2 input pos. NOR Gate	74LS02
UE7	Binary w/Clear Synchronous Up/Down Dual Clock Counter	74LS193
UF2	Hex Inverter Buffer/Driver	7406
UF3	Triple 3 input pos. NAND Gate	74LS10
UF4	Binary w/Clear Synchronous Up/Down Dual Clock Counter	74LS193
UF5	Quad 2 input pos. NAND Gate	74LS00
UF6	Dual-D Flip-Flop	74LS74
UG1	Hex Schmitt-Trigger INverter	74LS14
UG2	Quad 2 input EXCLUSIVE-OR Gate	74LS86
UG3	Dual Retriggerable Resettable Monostable Multivibrator	9602
UG4	Hex Buffer/Driver	7417
UH4	Comparator w/Open Collector Output	LM311
UH5	Differential Video Amplifier	NE592N
UH7	Differential Video Amplifier	NE592N
Y1	Crystal	16 MHz

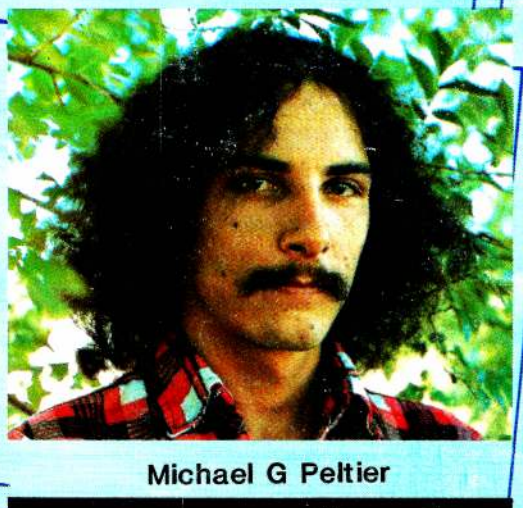
Drive Motor/Servo Circuit

Designator	Description	Value/Part number
C1	Capacitor	10uF,35V
C2	Capacitor	4700pF
C3	Capacitor	-----
C4	Capacitor	0.47uF,35V
C5	Capacitor	10uF,35V
C6	Capacitor	10uF,35V
C7	Capacitor	0.47uF,35V
C8	Capacitor	0.063uF
C9	Capacitor	0.47uF,35V
CR1	Diode	1N4148
CR2	Diode	1N4148
CR3	Diode	1N4148
CR4	Diode	1N4148
CR5	Diode	1N4148
IC1	Speed Controller	SONY 2463
Q1	Transistor	25C2785
Q2	Transistor	25C2785
Q3	Transistor	25A1015
Q4	Transistor	25B569
R1	Resistor	10K
R2	Resistor	68K
R3	Resistor	220
R4	Resistor	3.3K
R5	Resistor	2.7K
R6	Resistor	820
R7	Resistor	10K
R8	Resistor	150
R9	Resistor	----
R10	Resistor	3.32K
VR1	Variable Resistor	----

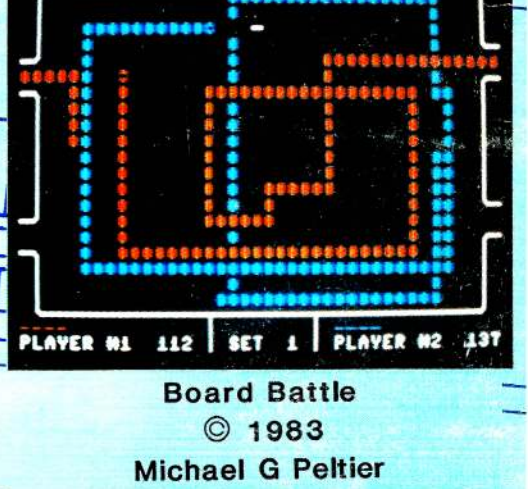
About The Author

Mr. Peltier is an electronics technician, technical writer, inventor of electronics devices, and designer of video games such as Board Battle. (Board Battle, shown at the right, is available internationally through GOSUB OF SLIDELL, INC., and affiliated distributors.)

After experiencing an electronic failure in his personal VIC-1541, Mr. Peltier discovered there was no documentation available to guide him in its repair. Therefore, he undertook to publish a manual that would enable others to repair their own units.



Michael G Peltier



Board Battle
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Michael G Peltier

About The Manual

How to do your own maintenance . . . troubleshooting . . . schematics . . . theory of operation . . . cleaning hints . . . conversion from one power source to another . . . calibration. These topics and many more will make this manual a valued addition to your reference shelf.

Whether you are an amateur electronics technician or a seasoned professional, you will be able to realize the full potential of your VIC-1541 by using this manual. Step-by-step instructions will lead you through the proper methods to get your VIC-1541 up and going again in a hurry.

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